

1. Introduction

This technical note is intended to provide information about the proper power-on procedure for Kionix **KX132** and **KX134** family accelerometers.

Proper functioning of power-on reset (POR) is dependent on the specific **VDD**, **VDD_{LOW}**, **T_{VDD}** (rise time), and **T_{VDD_OFF}** profile of individual applications. It is recommended to minimize **VDD_{LOW}**, and **T_{VDD}**, and maximize **T_{VDD_OFF}**. It is also advised that the VDD ramp up time **T_{VDD}** be monotonic. To assure proper POR in all environmental conditions the application should be evaluated over the customer specified range of **VDD**, **VDD_{LOW}**, **T_{VDD}**, **T_{VDD_OFF}** and temperature as POR performance can vary depending on these parameters

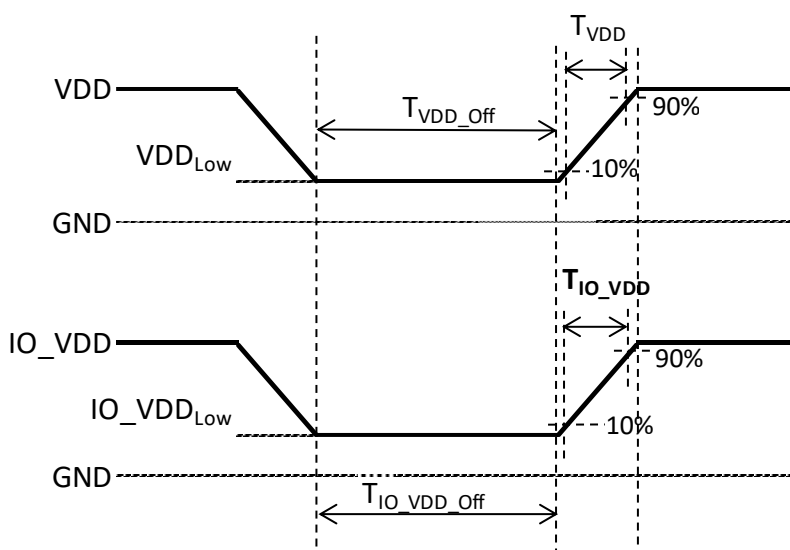


Figure 1: Power-On Reset Timing Diagram

2. POR Performance

Bench Testing has demonstrated POR performance regions for a proper POR trigger. To assure POR trigger properly executes, setting operational thresholds consistent with Table 1 is recommended.

| Parameters | Units | Min | Typical | Max |
|---|-------|-----|---------|-----|
| VDD rise time: $T_{VDD}^{1,2,3}$ | ms | | | 5 |
| IO_VDD rise time: $T_{IO_VDD}^{1,2,3}$ | ms | | | 5 |
| VDD off time: $T_{VDD_OFF}^{4,6}$ | ms | 20 | | |
| IO_VDD off time: $T_{IO_VDD_OFF}^{4,6}$ | ms | 20 | | |
| VDD low voltage: $VDD_{Low}^{4,6}$ | mV | | | 200 |
| IO_VDD low voltage: $IO_VDD_{Low}^{4,6}$ | mV | | | 200 |
| Software Reset Time ⁶ | ms | 2 | | |
| Power Up Time ⁷ | ms | | 20 | 50 |

Table 1: POR Performance

Notes:

1. VDD and IO_VDD must always be monotonic ramps without ambiguous state
2. T_{VDD} and T_{IO_VDD} rise from 10% to 90% of final value needs to be ≤ 5 ms.
3. IO_VDD amplitude must remain $\leq VDD$.
4. T_{VDD_OFF} and $T_{IO_VDD_OFF}$ are off time for VDD and IO_VDD rails respectively. In order to prevent the accelerometer from entering an ambiguous state, both VDD and IO_VDD need to be pulled down to GND (≤ 200 mV) for duration of time ≥ 20 ms.
5. It is important the user determines the timing (T_{VDD_OFF}) and threshold (VDD_{Low}) levels by evaluating the performance in the specific system for which the device will be incorporated.
6. Software Reset Time is defined as time it takes to perform a RAM reboot routine following the setting of SRST bit to 1 in the CNTL2. The SRST bit will remain 1 until the RAM reboot routine is completed.
7. Power Up Time is defined as time from VDD and IO_VDD become valid to device boot completion.

3. Software Reset

Issuing the Software Reset command after the device was powered up is recommended. This is effective against dynamic or non-linear behavior of a power supply or unexpected noise above normal on the power rail during a power up.

3.1. I²C Interface

3.1.1. I²C Slave Addresses for Software Reset

The Software Reset command may need to be sent to **two** I²C slave addresses. The 7-bit slave address associated with the KX132 and KX134 family of accelerometers is 00111YX, where the user programmable bit X, is determined by the assignment of ADDR (pin 1) to GND or IO_VDD. The factory programmable bit Y is set at the factory. An unsuccessful power-on may cause the internal value of the programmable bit Y to be flipped from 0 to 1 or 1 to 0. As a result, the user will need to take this into account and possibly send the required commands to the ‘flipped’ I²C address if attempts to send to the ‘primary’ address have failed. The Table 2 shows the ‘primary’ and ‘flipped’ 7-bit slave addresses for devices with ADDR pin connected to IO_VDD.

| Description | Address Pad | 7-bit Address | <7> | <6> | <5> | <4> | <3> | Y | X |
|----------------------------------|-------------|---------------|-----|-----|-----|-----|-----|-----|-----|
| | | | | | | | | <2> | <1> |
| I ² C Primary Address | IO_VDD | 0x1F | 0 | 0 | 1 | 1 | 1 | 1 | 1 |
| I ² C Flipped Address | | 0x1D | 0 | 0 | 1 | 1 | 1 | 0 | 1 |

Table 2: I²C Primary and Flipped 7-bit Slave Addresses with ADDR pin (X) at IO_VDD

The Table 3 shows the ‘primary’ and ‘flipped’ 7-bit slave addresses for devices with ADDR pin connected to GND.

| Description | Address Pad | 7-bit Address | <7> | <6> | <5> | <4> | <3> | Y | X |
|----------------------------------|-------------|---------------|-----|-----|-----|-----|-----|-----|-----|
| | | | | | | | | <2> | <1> |
| I ² C Primary Address | GND | 0x1E | 0 | 0 | 1 | 1 | 1 | 1 | 0 |
| I ² C Flipped Address | | 0x1C | 0 | 0 | 1 | 1 | 1 | 0 | 0 |

Table 3: I²C Primary and Flipped 7-bit Slave Addresses with ADDR pin (X) at GND

3.1.2. Software Reset Sequence following Power Up

- a. Following the power up, write 0x00 to internal register 0x7F using I²C Primary Address as specified in Table 2 or Table 3 depending of the connection of ADDR pin. If command was acknowledged (ACK received), proceed to the next step while addressing the device using I²C Primary Address. If ACK was not received, resend the command using I²C Flipped Address. If command was acknowledged, proceed to the next step while addressing the device using I²C Flipped Address. If command was not acknowledged again, the device should be power cycled.

| Register Name | Address | Value |
|---------------|---------|-------|
| 0x7F | 0x7F | 0x00 |

- b. Write 0x00 to Control Register 2 (CNTL2). If NACK received, the device should be power cycled.

| Register Name | Address | Value |
|---------------|---------|-------|
| CNTL2 | 0x1C | 0x00 |

- c. Write 0x80 to Control Register 2 (CNTL2) to initiate software reset, which performs the RAM reboot routine. If software reset command was acknowledged (ACK received), wait for the duration of time specified in Table 1 for completion of the Software Reset and proceed to the next step. If NACK received, the device should be power cycled.

| Register Name | Address | Value |
|---------------|---------|-------|
| CNTL2 | 0x1C | 0x80 |

- d. Read content of “Who am I” register (WHO_AM_I) using the I²C Primary Address. If value read is what is expected, proceed to the next step. If not, the software reset has failed and the device should be power cycled.

| Part | Register Name | Address | Value |
|-------|---------------|---------|-------|
| KX132 | WHO_AM_I | 0x13 | 0x3D |
| KX134 | WHO_AM_I | 0x13 | 0x46 |

Table 4: Expected Value of Who_Am_I register for KX132 & KX134 Accelerometers

- e. Read the content of COTR register. If read value is 0x55, the device operation can be started. If read value is not 0x55, the software reset has failed and the device should be power cycled.

| Register Name | Address | Value |
|---------------|---------|-------|
| COTR | 0x12 | 0x55 |

3.1.3. Software Reset Timing Diagram

Figure 2 below shows an example of executing Software Reset sequence outlined section 3.1.2 following a power up. The first attempt is to communicate with device using I²C Primary Address as specified in Table 2 or Table 3 depending of the connection of ADDR pin. If attempt is unsuccessful, the second attempt is to communicate with device using I²C Flipped Address mentioned in the same tables. Please wait for the duration of time specified in Table 1 for completion of the Software Reset before proceeding.

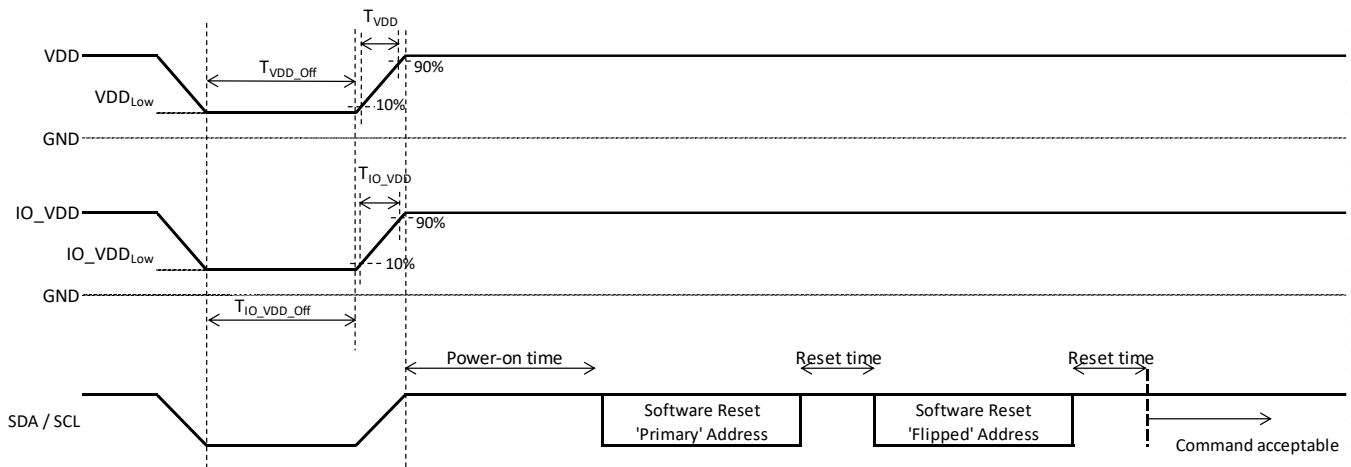


Figure 2: Power-On Timing Diagram followed by sending of two I²C Software Reset Commands

3.2. SPI Interface

3.2.1. Software Reset Sequence following Power Up

- a. Following the power up, write 0x00 to internal register 0x7F

| Register Name | Address | Value |
|---------------|---------|-------|
| 0x7F | 0x7F | 0x00 |

- b. Write 0x00 to Control Register 2 (CNTL2)

| Register Name | Address | Value |
|---------------|---------|-------|
| CNTL2 | 0x1C | 0x00 |

- c. Write 0x80 to Control Register 2 (CNTL2) to initiate software reset, which performs the RAM reboot routine.

| Register Name | Address | Value |
|---------------|---------|-------|
| CNTL2 | 0x1C | 0x80 |

- d. Wait for the duration of time specified in Table 1 for completion of the Software Reset before proceeding.
- e. Read content of “Who am I” register (WHO_AM_I). If value read is what is expected, proceed to the next step. If not, the software reset has failed and the device should be power cycled.

| Part | Register Name | Address | Value |
|-------|---------------|---------|-------|
| KX132 | WHO_AM_I | 0x13 | 0x3D |
| KX134 | WHO_AM_I | 0x13 | 0x46 |

Table 5: Expected Value of Who_Am_I register for KX132 & KX134 Accelerometers

- f. Read the content of COTR register. If read value is 0x55, the device operation can be started. If read value is not 0x55, the software reset has failed and the device should be power cycled.

| Register Name | Address | Value |
|---------------|---------|-------|
| COTR | 0x12 | 0x55 |

3.2.2. Software Reset Timing Diagram

Figure 3 below shows an example of sending Software Reset following the initial power on. Please wait for the duration of time specified in Table 1 for completion of the Software Reset before proceeding.

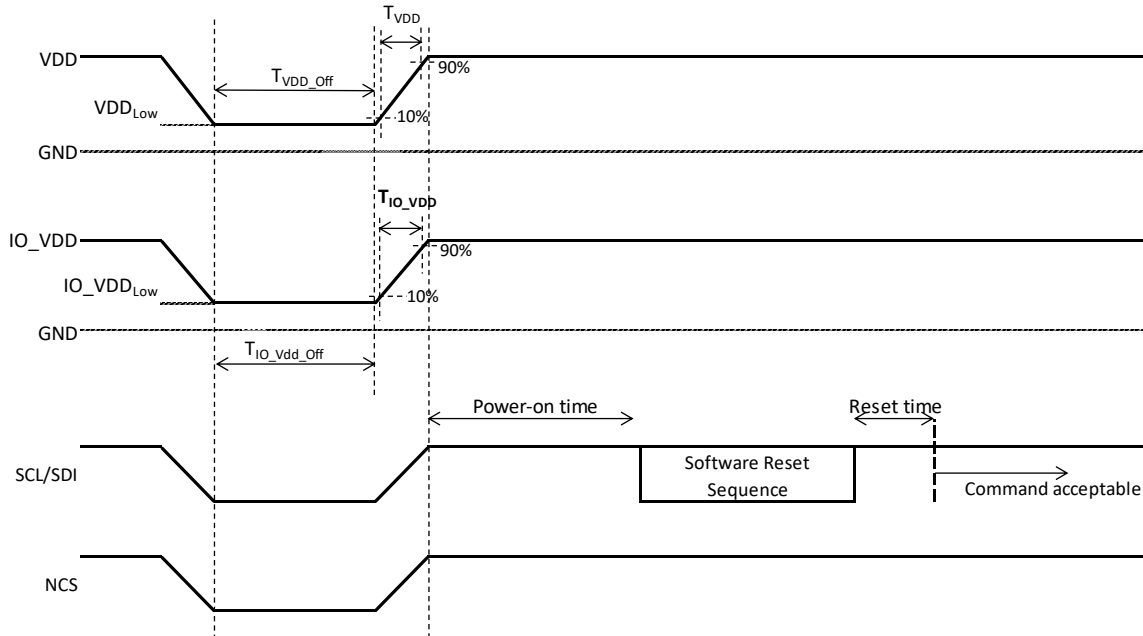


Figure 3: Power-On Timing Diagram followed by sending Software Reset Commands

The data provided by Kionix is intended for initial customer design guidance only. Kionix POR testing looks at a finite number of test configurations. Each customer application will have varying input sensor parameters (electrical, mechanical, and environmental) that will be different than the configurations tested by Kionix. Each customer utilizing the sensor will need to properly validate the sensor (including POR function) within their application under their specific use cases to ensure it responds as required.