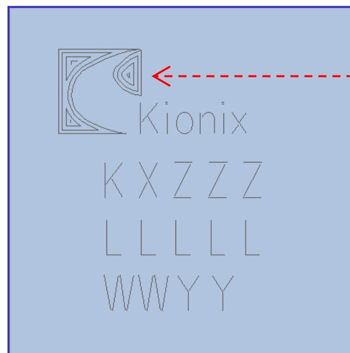
## Introduction

This technical note is intended to provide information about Kionix's 5 x 5 mm DFN (non wettable flank, i.e. standard) packages and guidelines for developing PCB land pattern layouts. These guidelines are general in nature and based on recommended industry practices. The user must apply their actual experiences and development efforts to optimize designs and processes for their manufacturing techniques and the needs of varying end-use applications. It should be noted that with the proper PCB footprint and solder stencil designs, the package will self-align during the solder reflow process.

## Package Marking




- Marking font type : Arial
- Font size : 1.5 Point (0.56 mm height)
- Line space : 0.3 mm
- Text information :
  - 1st line – Logo. May be used as Pin 1 indicator. No additional dot type pin#1 mark.
  - 2nd line – Device name
  - 3rd line – Assembly Build Lot code
  - 4th line – Date code (WWYY)

Note - 2nd ~ 4th line text shall be left justified.

**Figure 1:** 5x5 DFN Package Marking Information

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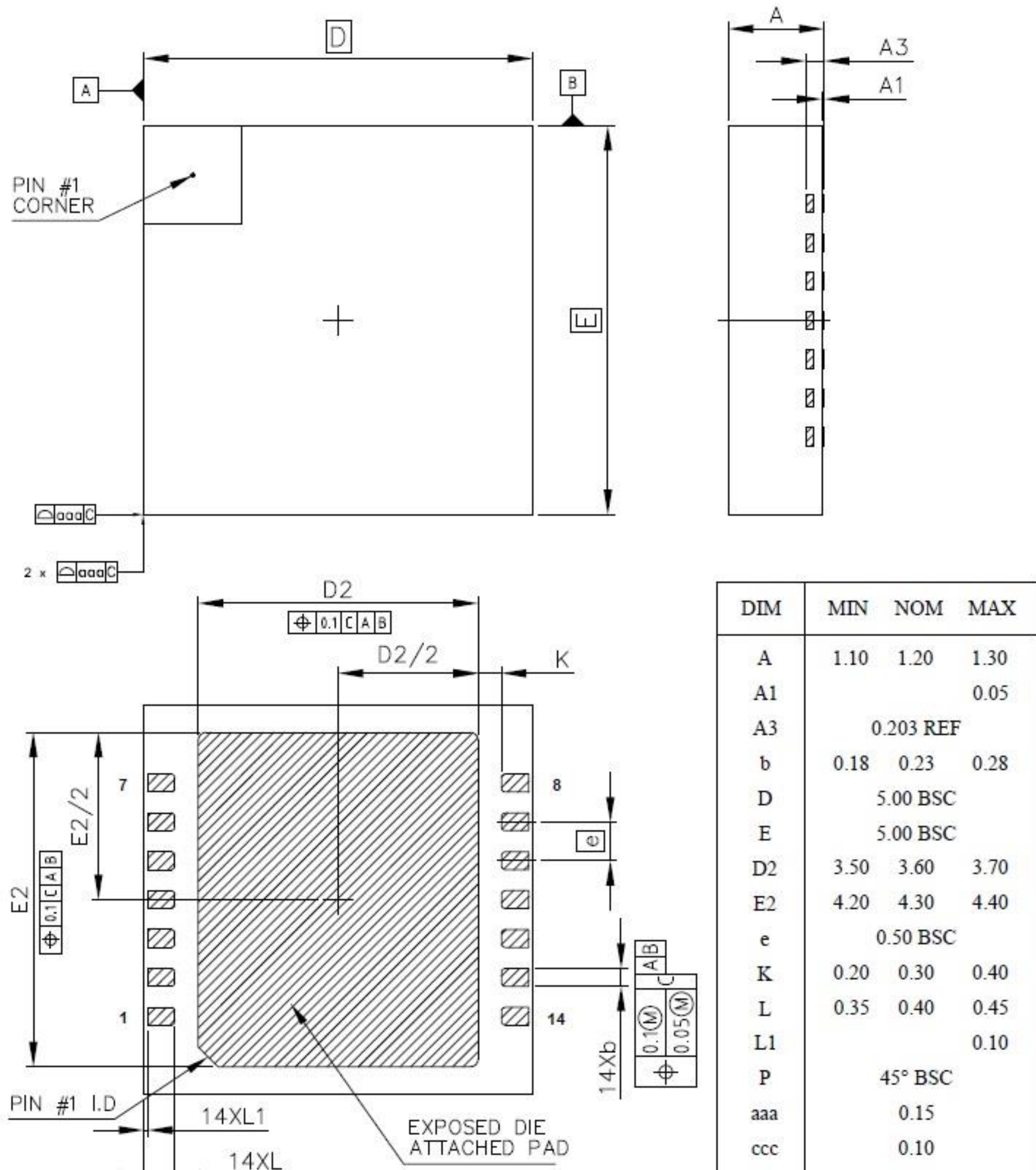
## Package Outline and Dimensions

The following diagrams show the outline of the 5 x 5 DFN packages with dimensions and tolerances. All dimensions and tolerances conform to ASME Y14.5M-1994. All dimensions are in millimeters and angles are in degrees.




| DIM | MIN | NOM | MAX |
|---|---|---|---|
| A | 1.10 | 1.20 | 1.30 |
| A1 | | | 0.05 |
| A3 | | 0.203 REF | |
| b | 0.18 | 0.23 | 0.28 |
| D | | 5.00 BSC | |
| E | | 5.00 BSC | |
| D2 | 3.50 | 3.60 | 3.70 |
| E2 | 4.20 | 4.30 | 4.40 |
| e | | 0.50 BSC | |
| K | 0.20 | 0.30 | 0.40 |
| L | 0.35 | 0.40 | 0.45 |
| L1 | | | 0.10 |
| P | | 45° BSC | |
| aaa | | 0.15 | |
| ccc | | 0.10 | |

**Figure 2:** 5 x 5 x 1.2 mm Package Outline Drawing

*Note: “Pin 1 Corner” indicator is shown for reference only

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## PCB Layout Recommendations

Given the above package dimensions, the following guidelines are recommended:

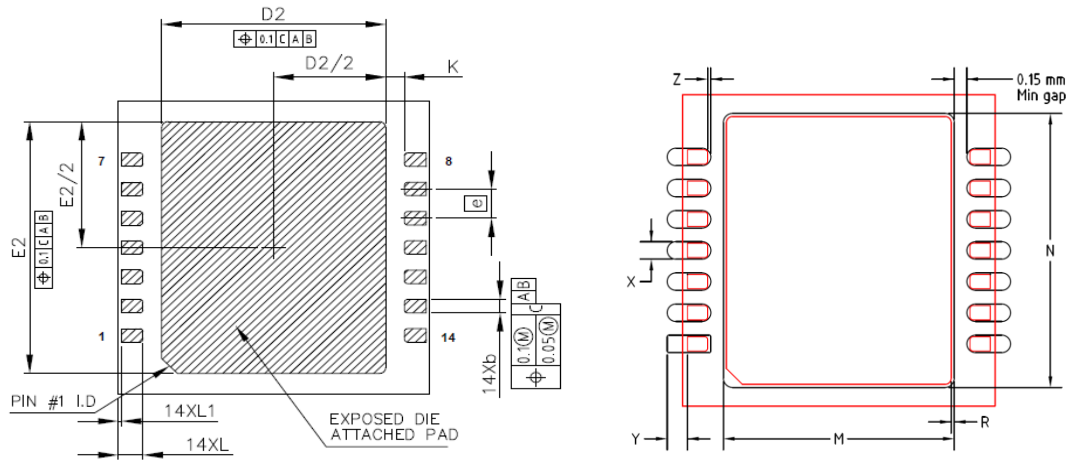


**Figure 3:** Package Outline Drawing (Left) vs PCB Land Pattern Layout (Right); (Bottom view)

| Nominal Package **I/O Pad** Dimensions (mm) | | | PCB **I/O Pad** Dimension Guidelines (mm) | | |
|---|---|---|---|---|---|
| Pad Pitch (e) | Pad Width (b) | Pad Length (L-L1) | Pad Width (X) | Outward Extension (y) | Inward Extension (z) |
| 0.5 | 0.23 | 0.3 | 0.28 Nom | 0.15 Min | 0.05 Min |

The perimeter PCB I/O pads are slightly larger on all sides than the package I/O pads. The outward extension (y) of the I/O pads can be increased beyond the 0.15 mm minimum, when PCB area is available. However, any increase in the inward extension (z) must consider the effect on the isolation gap to the center pad. This gap must not be less than 0.15 mm to avoid shorting.

| Nominal Package **Center Pad** Dimensions (mm) | | | PCB **Center Pad** Dimension Guidelines (mm) | | |
|---|---|---|---|---|---|
| | Pad Width (D2) | Pad Length (E2) | Pad Width (M) | Pad Length (N) | Outward Extension (R) |
| 5 x 5 x 1.2 | 3.6 | 4.3 | 3.6 | 4.3 | 0 - 0.15 Max |

The center pad should be designed 0 mm to 0.15 mm larger per side than the package's exposed center pad. An example of a PCB land pattern is shown in Figure 4.

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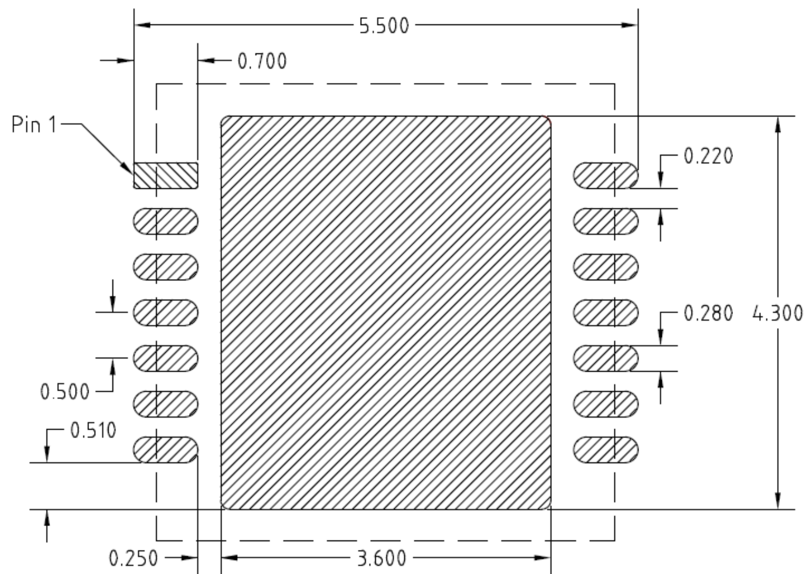


**Figure 4:** Example of a PCB land pattern for the 5 x 5 x 1.2 mm DFN package
(Top view)

Using a 0.0508 mm solder mask around each pad (pad dimension + 0.1016 mm), the minimum solder mask web is 0.1484 mm between perimeter I/O and center pads and 0.1184 mm between perimeter I/O pads.

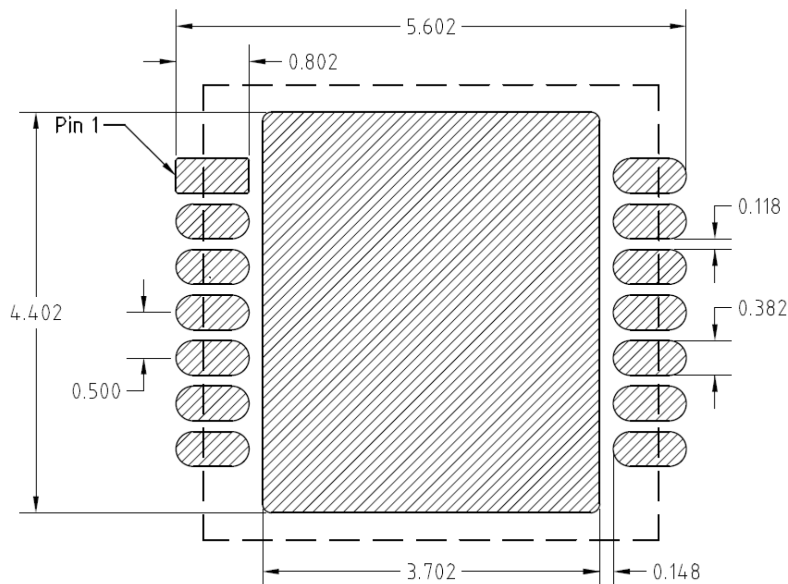


**Figure 5:** Example of solder mask for the 5 x 5 x 1.2 mm DFN package
(Top view)


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## Solder Stencil Guidelines

A laser-cut, stainless steel stencil with electro-polished trapezoidal walls is recommended. The recommended solder stencil thickness is 0.127 mm.

Re-flowed solder joints on the PCB perimeter I/O pads should have about a 50 to 75 µm (2 to 3 mil) standoff height. To achieve this, the stencil aperture size-to-pad size should typically be a 1:1 ratio.

To reduce solder paste volume on the center pad, it is recommended that an array of smaller apertures be used instead of one large aperture. The smaller apertures can be circular or square and of various dimensions and array sizes. The main goal should be a dimensional combination that results in a 40% - 80% solder paste coverage. This reduced coverage on the center pad is important in achieving good coverage without excessive standoff or bridging to the PCB perimeter I/O pads. An example layout is given in Figure 6.

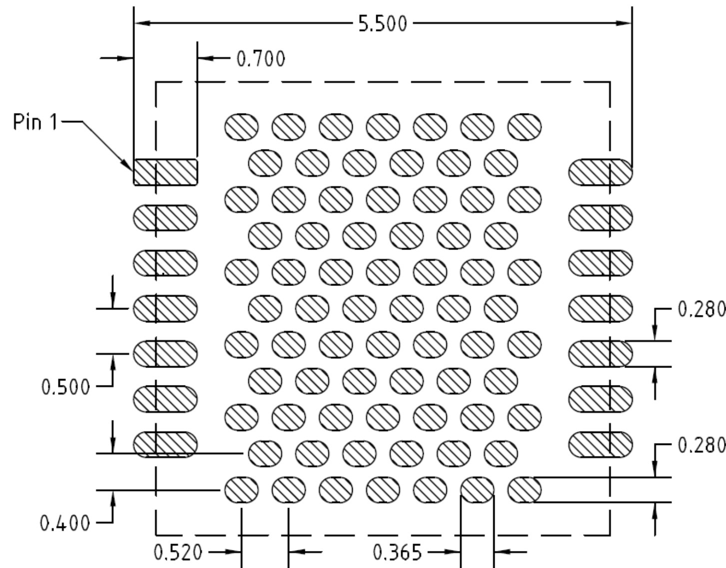


**Figure 6:** Example of a 5 x 5 x 1.2 mm DFN solder stencil layout;
40% coverage on center pad.
(Top view)

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## PCB Via and Trace Placement

Vias are not needed for thermal dissipation, as our part doesn't generate much heat. Therefore, only electrical vias are needed. If vias are not in the pads; capped, plugged, tented, un-capped, or un-plugged vias can be used.

To ensure optimal performance, vias and traces should not be placed on the top layer directly beneath the accelerometer. The accelerometer should be mounted over a ground plane to minimize EMI from other signals. In the case PCB assemblies are stacked, there should be a ground plane over the accelerometer for the same reason.

The following figures illustrate an example of proper PCB via and trace placement. Obviously, each product will present its own physical limitations for accelerometer placement and trace routing. Therefore, these guidelines are general in nature. Engineering judgment should be used to try to avoid metal placement directly beneath the sensor on the same layer.

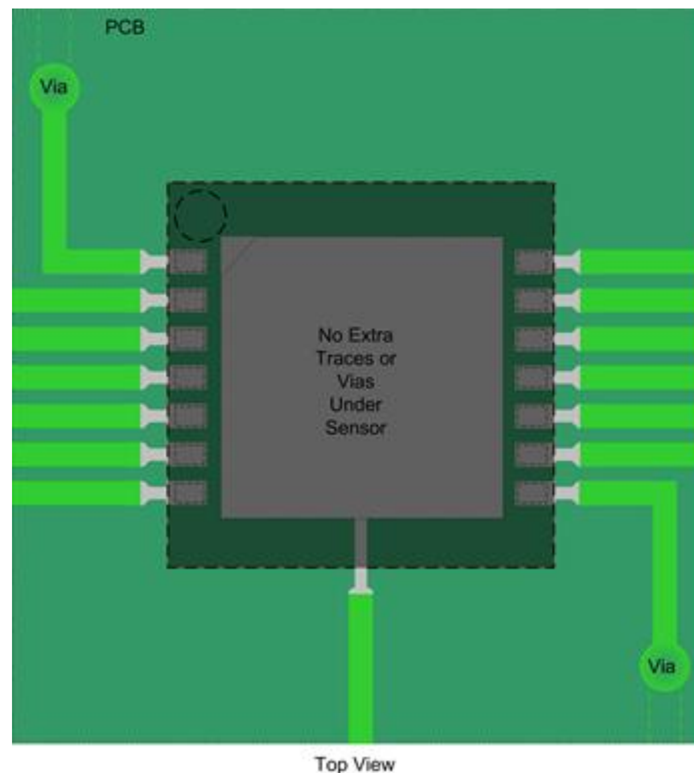


**Figure 7:** Via and Trace “Keep-out”
(Top View)

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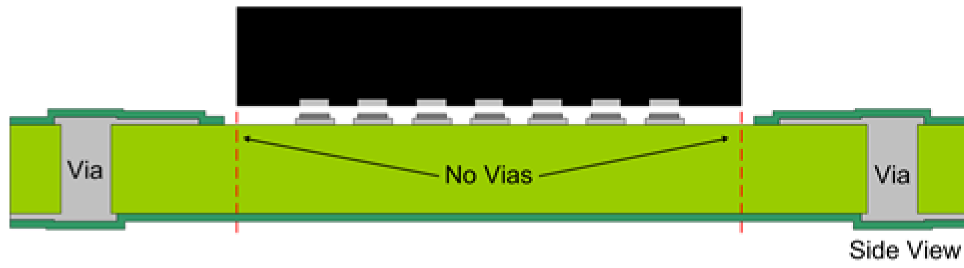


**Figure 8:** Via and Trace "Keep-out"
(Side View)

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## Tape and Reel Dimensions

The following section provides information on the tape and reel used for shipping Kionix's 5 x 5 mm DFN accelerometers.

| Package | Tape Width | Component Pitch | Hole Pitch | Reel Diameter |
| --- | --- | --- | --- | --- |
| DFN (5x5) | 16mm | 8mm | 4mm | 330mm |

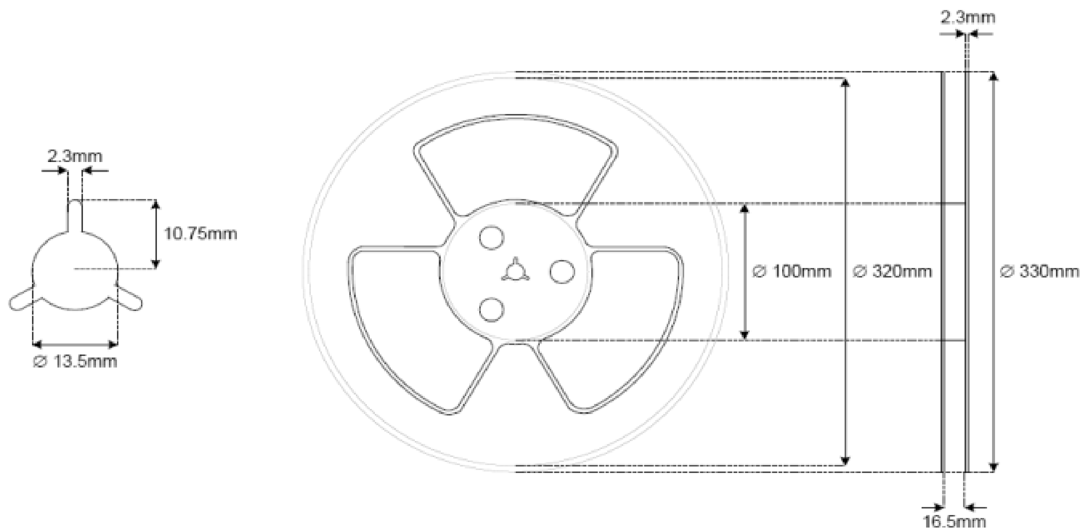


**Figure 9:** Dimensions of the Reel

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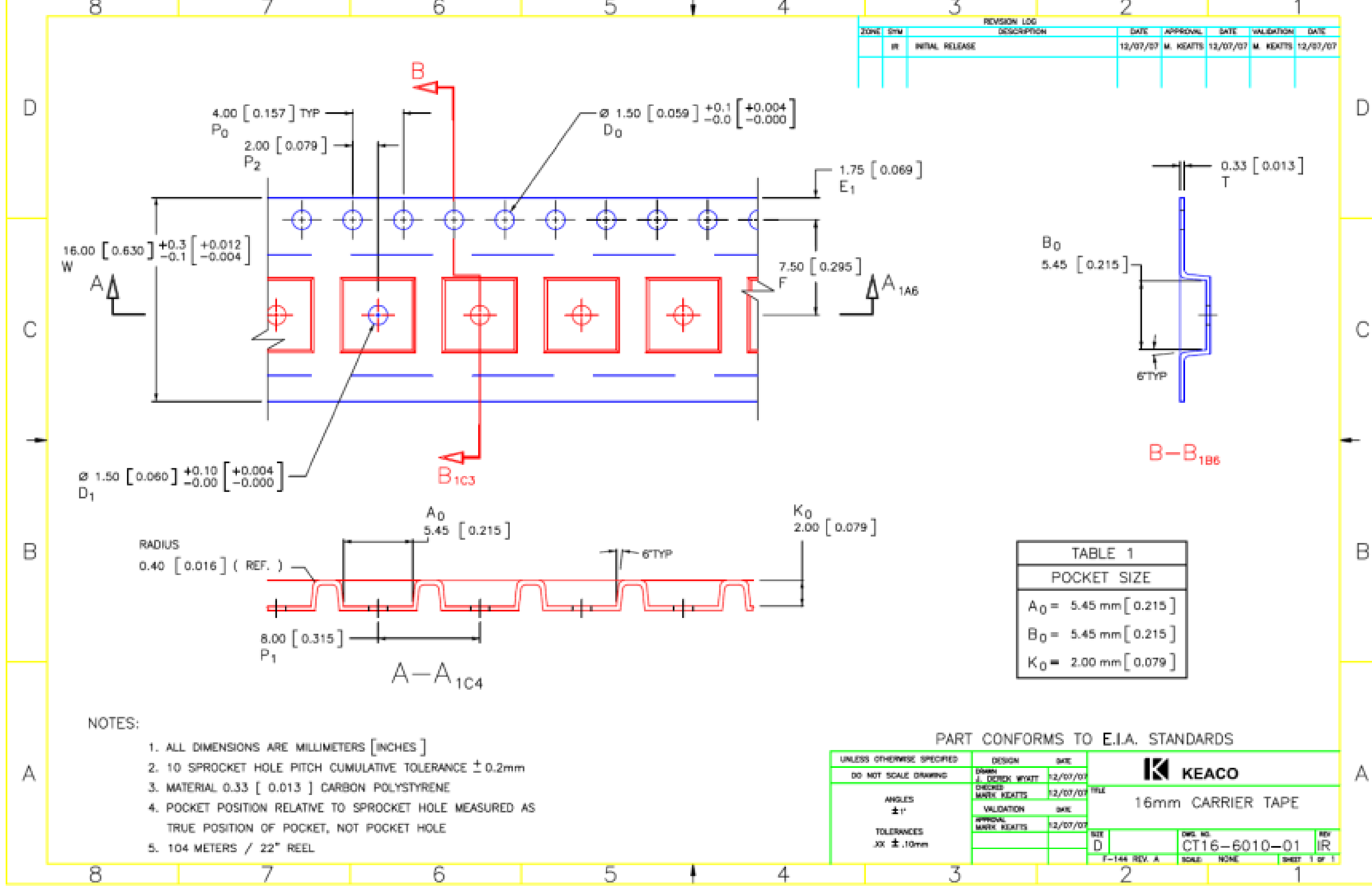


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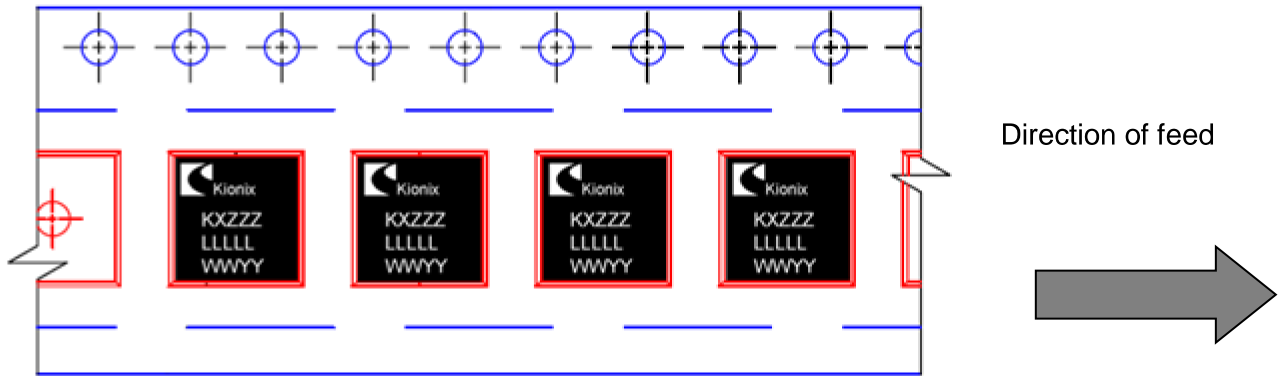


**Figure 10:** Orientation of the parts in the carrier tape and direction of feed


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## Revision History

| Rev | Date | Description of Change |
| --- | --- | --- |
| 1 | 01-Jul-2016 | Initial Release |
| 2 | 07-Nov-2017 | Updated Figure 3 (Package Outline Drawing vs Landing Pattern). Updated Figure 6 (DFN solder stencil layout).<br>Updated Package Marking section to clearly show Pin 1 indicator and added a note regarding Pin 1. |
| 3 | 13-Mar-2019 | Changed Figure 3 PCB Land Pattern Layout (Right) drawing to a new drawing.<br>Land was changed to pad where appropriate.<br>Nominal Package I/O Pad Dimensions: was changed to L - L1 or about 0.3.<br>Changed Figure 4 to current land design.<br>Added solder mask information.<br>Changed stencil thickness from 0.125mm to 0.127mm.<br>Changed Figure 6 to current stencil design; add % coverage.<br>PCB Via and Trace Placement: Add second paragraph.<br>Added Solder Stencil Figure 5. |


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