

Introduction

This technical note is intended to provide information about Kionix's 3 x 3 mm LGA packages and guidelines for developing PCB land pattern layouts. These guidelines are general in nature and based on recommended industry practices. The user must apply their actual experiences and development efforts to optimize designs and processes for their manufacturing techniques and the needs of varying end-use applications. It should be noted that with the proper PCB footprint and solder stencil designs, the package will self-align during the solder reflow process.

Package Marking



- Marking font type : Arial
- Font size : 1.5 Point (0.56 mm height)
- Line space : 0.1 mm
- Text information
 - 1st line – Device name
 - 2nd line – Assembly Build Lot code
 - 3rd line – Date code (WWYY)
 - 4th line – Pin #1 Dot (0.3 mm diameter)

Note - All text lines shall be right justified.

Figure 1. 3x3 mm LGA package marking information

Package Outline and Dimensions

The following diagrams show the package outline of one of the Kionix's sensors with dimensions and tolerances. **For actual package outline drawing of a specific part, see the corresponding product specification document.**

All dimensions and tolerances conform to ASME Y14.5M-1994. All dimensions are in millimeters and angles are in degrees. There may be variation in the location and shape of the "PIN 1 ID", for various product packages with the same pin layout.

10-pin LGA package

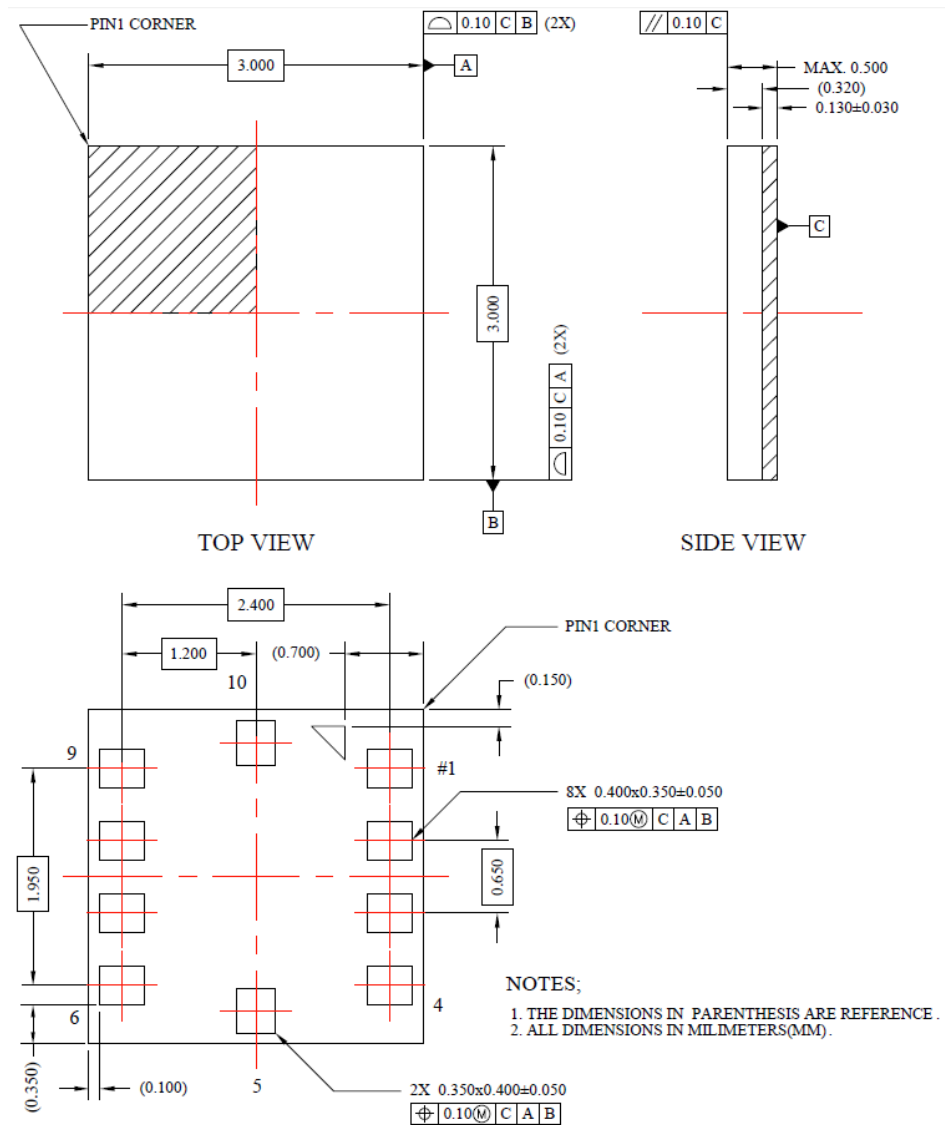


Figure 2. 10-pin 3 x 3 mm LGA package outline diagram with dimensions

16-pin LGA package

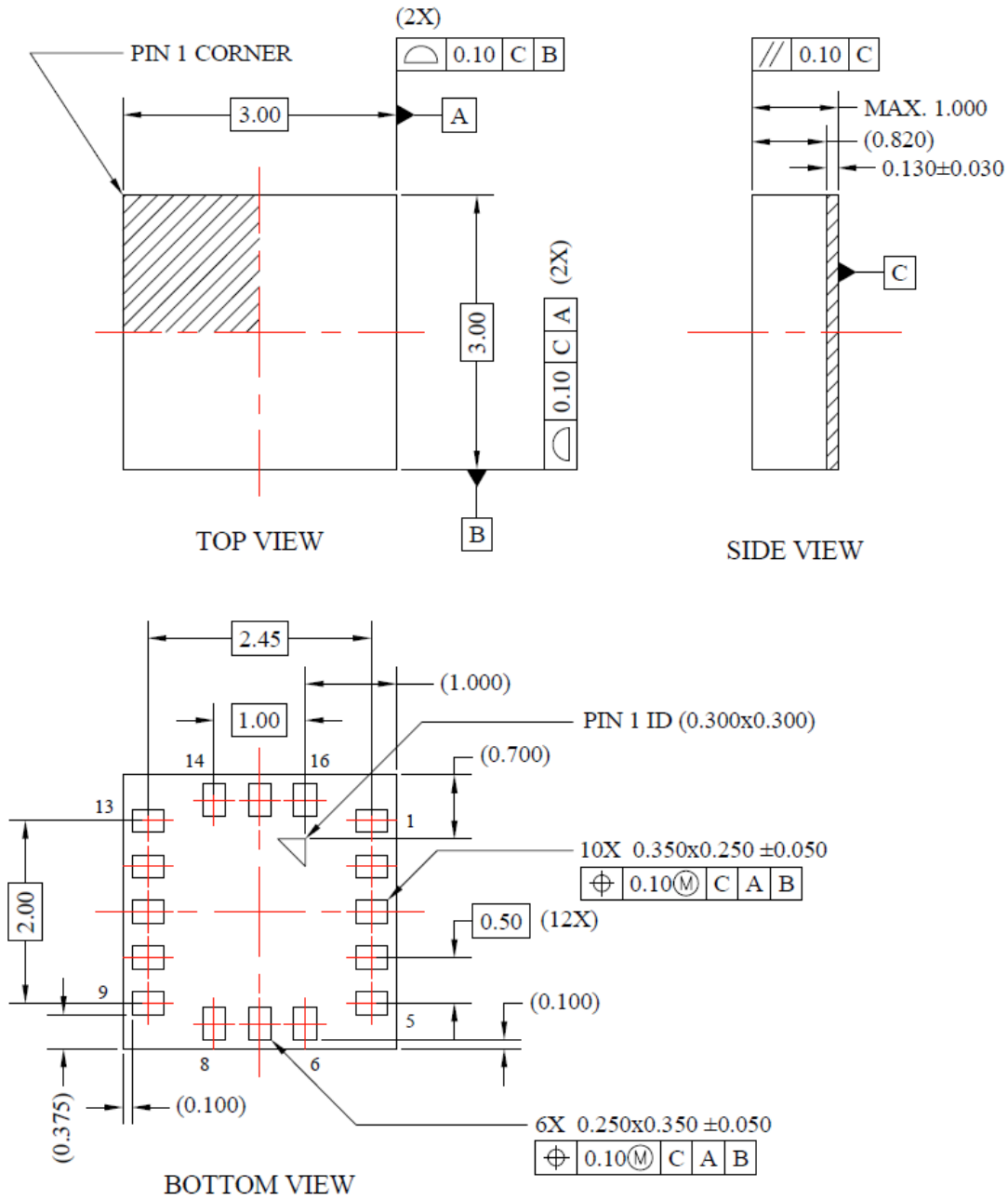


Figure 3. 16-pin 3 x 3 mm LGA package outline diagram with dimensions

Typical LGA packages expose metal traces on the package sides; so no solder material should be allowed to contact the package sides.

Solder Pad Layer Dimensions

The solder pocket is defined by dimensions of the metal layers behind the solder pad and the solder mask around the pad. There are two varieties of solder pad design in the Kionix 3x3 LGA.

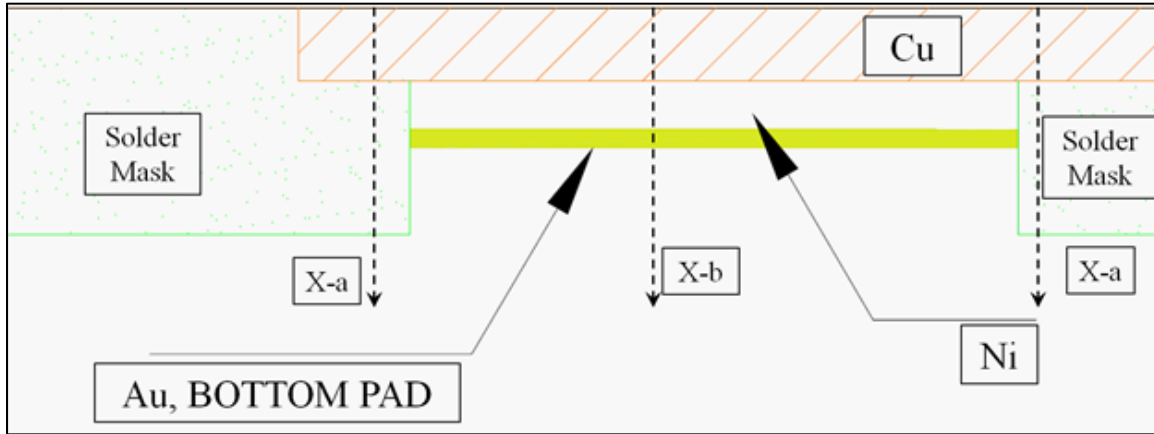


Table 1. For 3x3 products with 0.13mm substrates (KX023, KX23H, KXCJA)

Solder Mask (Cross Section "X-a")(μm)				Solder Pad (Cross section "X-b")(μm)			
Layer	Min	Nominal	Max	Layer	Min	Nominal	Max
S/M	10	20	30	NI	3	-	12
				Au	0.3	0.3	0.5*

* Absolute physical limit is 1.0 μm

Table 2. For 3x3 products with 0.21mm substrates (parts not in table 1)

Solder Mask (Cross Section "X-a")(μm)				Solder Pad (Cross section "X-b")(μm)			
Layer	Min	Nominal	Max	Layer	Min	Nominal	Max
S/M	15	30	45	NI	3	-	12
				Au	0.3	0.3	0.5*

* Absolute physical limit is 1.0 μm

PCB Layout Recommendations

Given the above 3 x 3 mm package dimensions, the following guidelines are recommended:

The PCB should be designed with NSMD (Non-Solder Mask Defined) openings for the LGA land pattern. The LGA land pattern should be an identical mirror image of the bottom pattern of the LGA package.

The pin 1 indicator triangle that is exposed on the LGA substrate does not need to be soldered to the PCB and should be left floating.

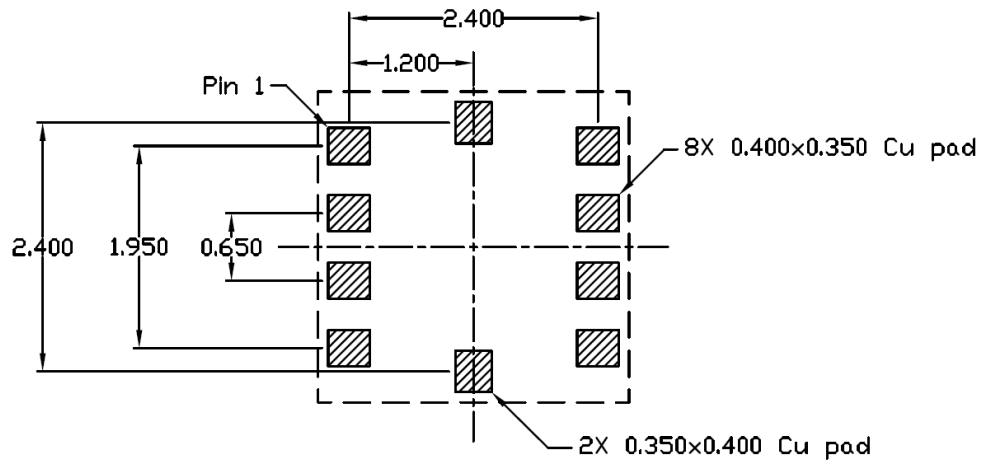


Figure 4: Example of a PCB land pattern for the 10-Pin 3 x 3 mm LGA package (Top view)

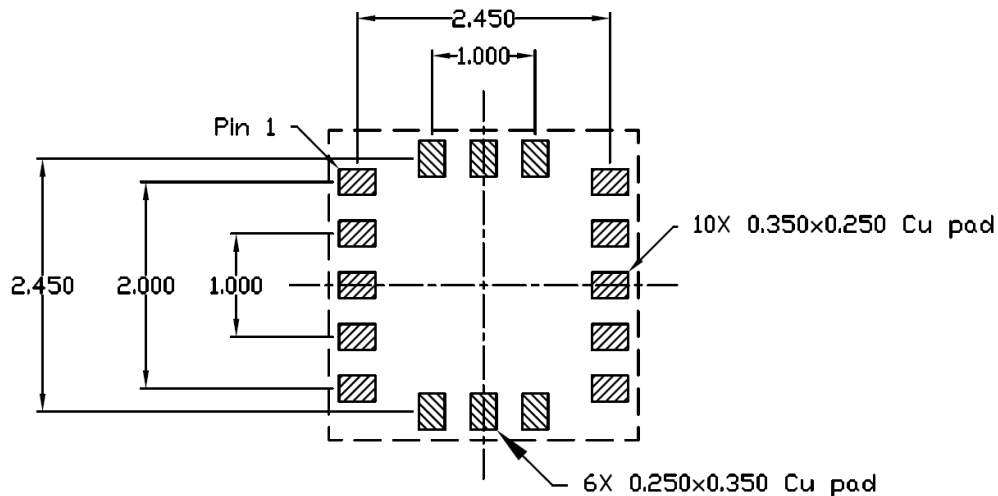


Figure 5: Example of a PCB land pattern for the 16-Pin 3 x 3 mm LGA package (Top view)

Using a 0.0635 mm solder mask around each pad (pad dimension + 0.1270 mm), the minimum solder mask web is 0.173 mm for the 10 Pin and 0.123 mm for the 16 Pin between I/O pads.

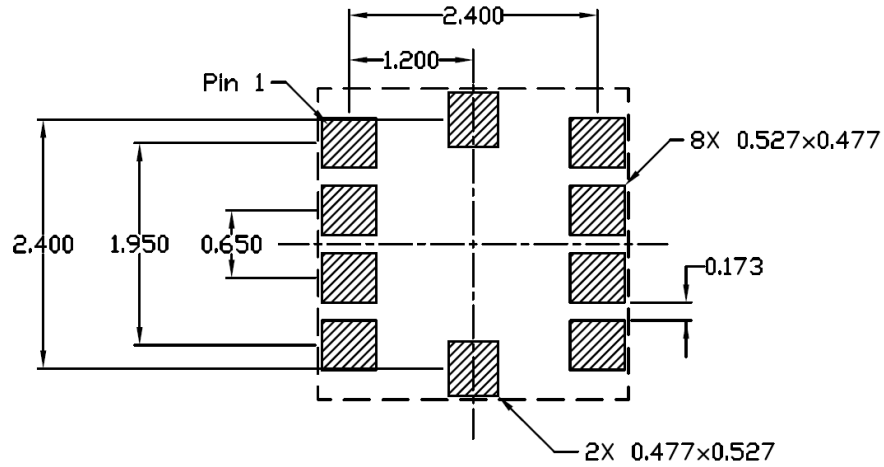


Figure 6: Example of solder mask for the 10 Pin 3 x 3 mm LGA package (Top view)

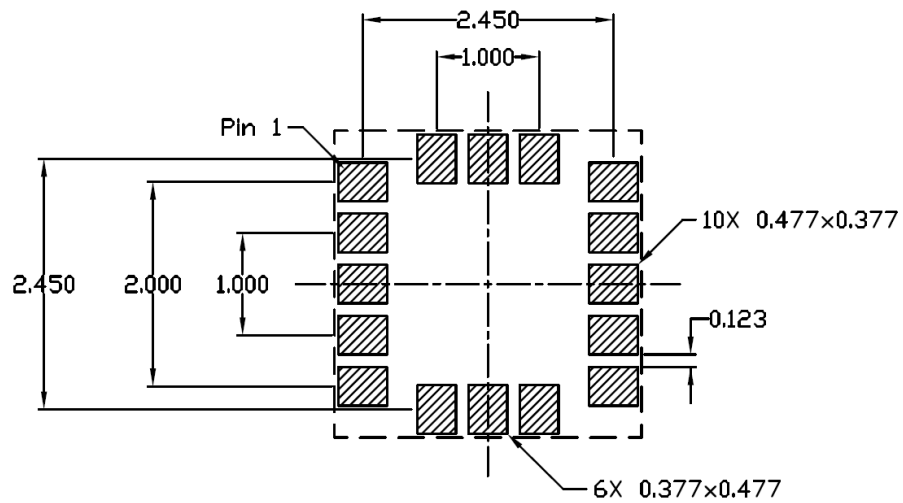


Figure 7: Example of solder mask for the 16 Pin 3 x 3 mm LGA package (Top view)

Solder Stencil Guidelines

A laser-cut, stainless steel stencil with electro-polished trapezoidal walls is recommended. The recommended solder stencil thickness is 0.127 mm for the 10-pin and 0.1016 mm for the 16-pin package. The solder mask openings should be an identical mirror image of the bottom pattern of the LGA package with a 0.025mm corner radius to improve paste release.

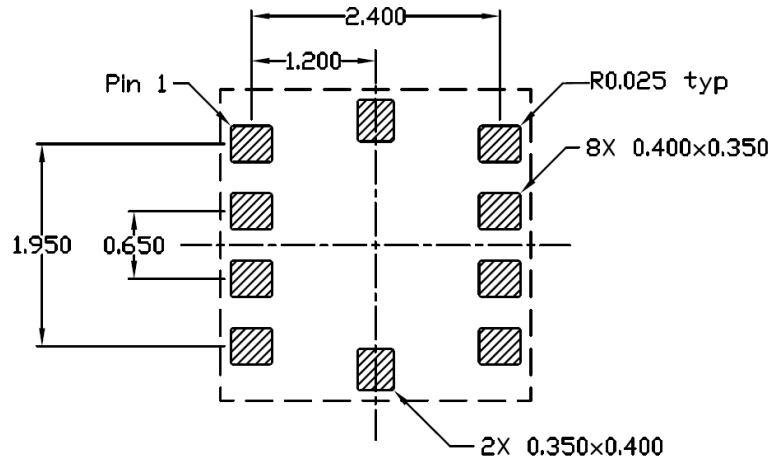


Figure 8: Example of a 10-pin 3 x 3 mm LGA solder stencil layout (Top view)

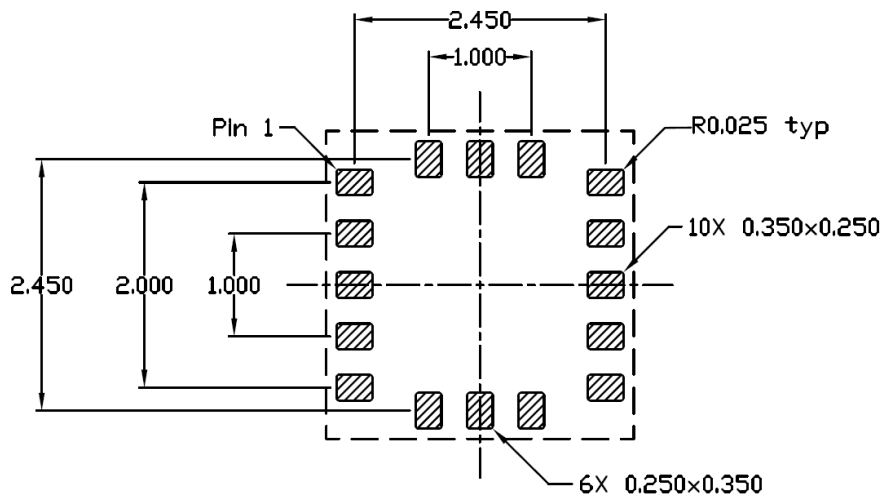


Figure 9. Example of a 16-pin 3 x 3 mm LGA solder stencil layout (Top view)

PCB Via and Trace Placement

Vias are not needed for thermal dissipation, as our part doesn't generate much heat. Therefore, only electrical vias are needed. If vias are not in the land pads, then capped, plugged, tented, un-capped or un-plugged vias can be used.

To ensure optimal performance, vias and traces should not be placed on the top layer directly beneath the sensor. The sensor should be mounted over a ground plane to minimize EMI from other signals. In the case PCB assemblies are stacked, there should be a ground plane over the sensor for the same reason.

The following figures illustrate an example of proper PCB via and trace placement. Obviously, each product will present its own physical limitations for sensor placement and trace routing. Therefore, these guidelines are general in nature. Engineering judgment should be used to try to avoid metal placement directly beneath the sensor on the same layer.

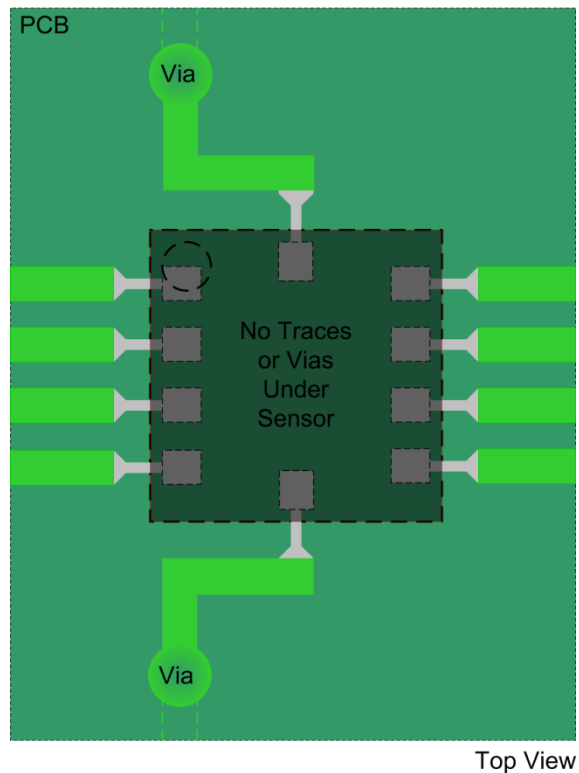


Figure 10. Via and Trace “Keep-out”
(Top View)

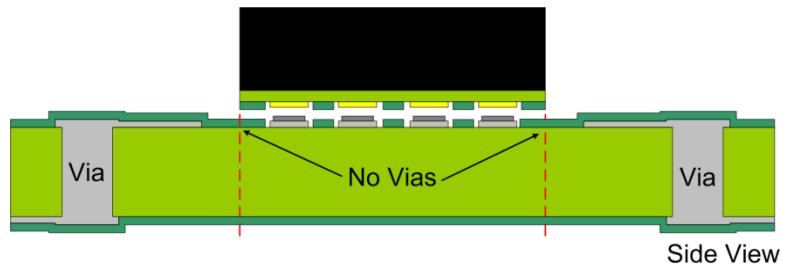


Figure 11. Via and Trace “Keep-out”
(Side View)

Tape and Reel Dimensions

The following section provides information on the tape and reel used for shipping Kionix's 3 x 3 mm LGA sensors.

Package	Tape Width	Component Pitch	Hole Pitch	Reel Diameter
LGA (3x3)	12mm	8mm	4mm	330mm

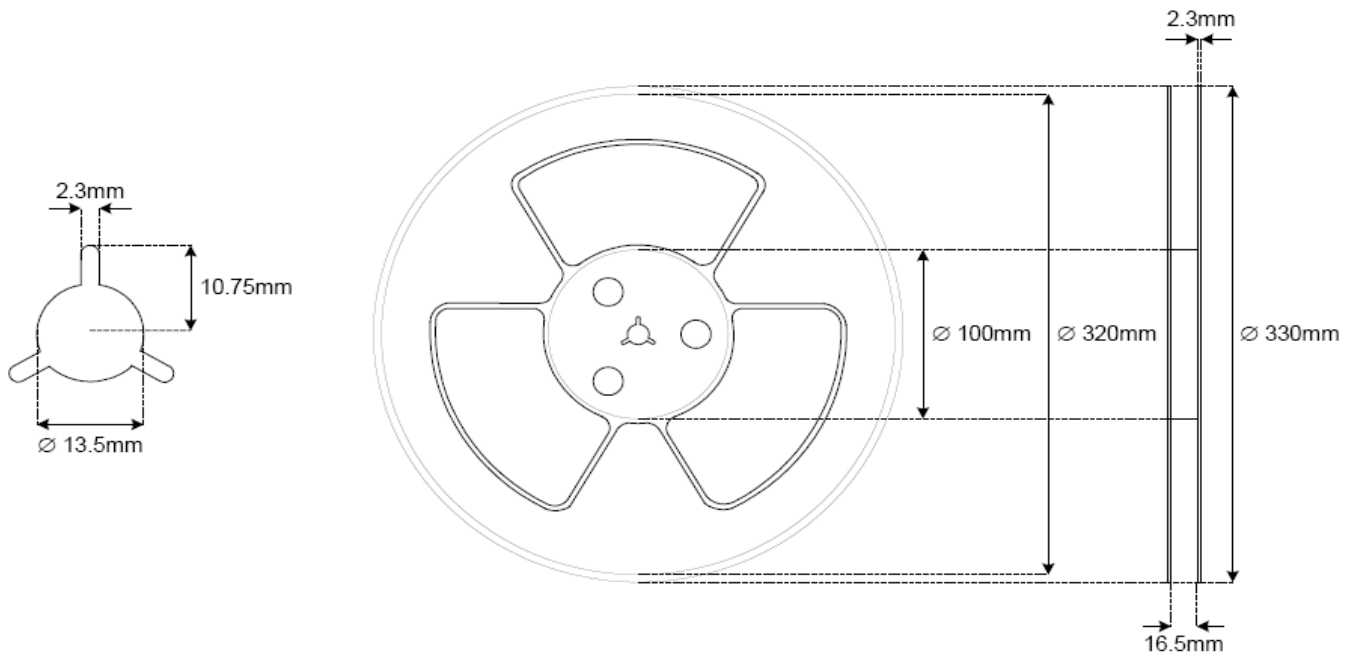
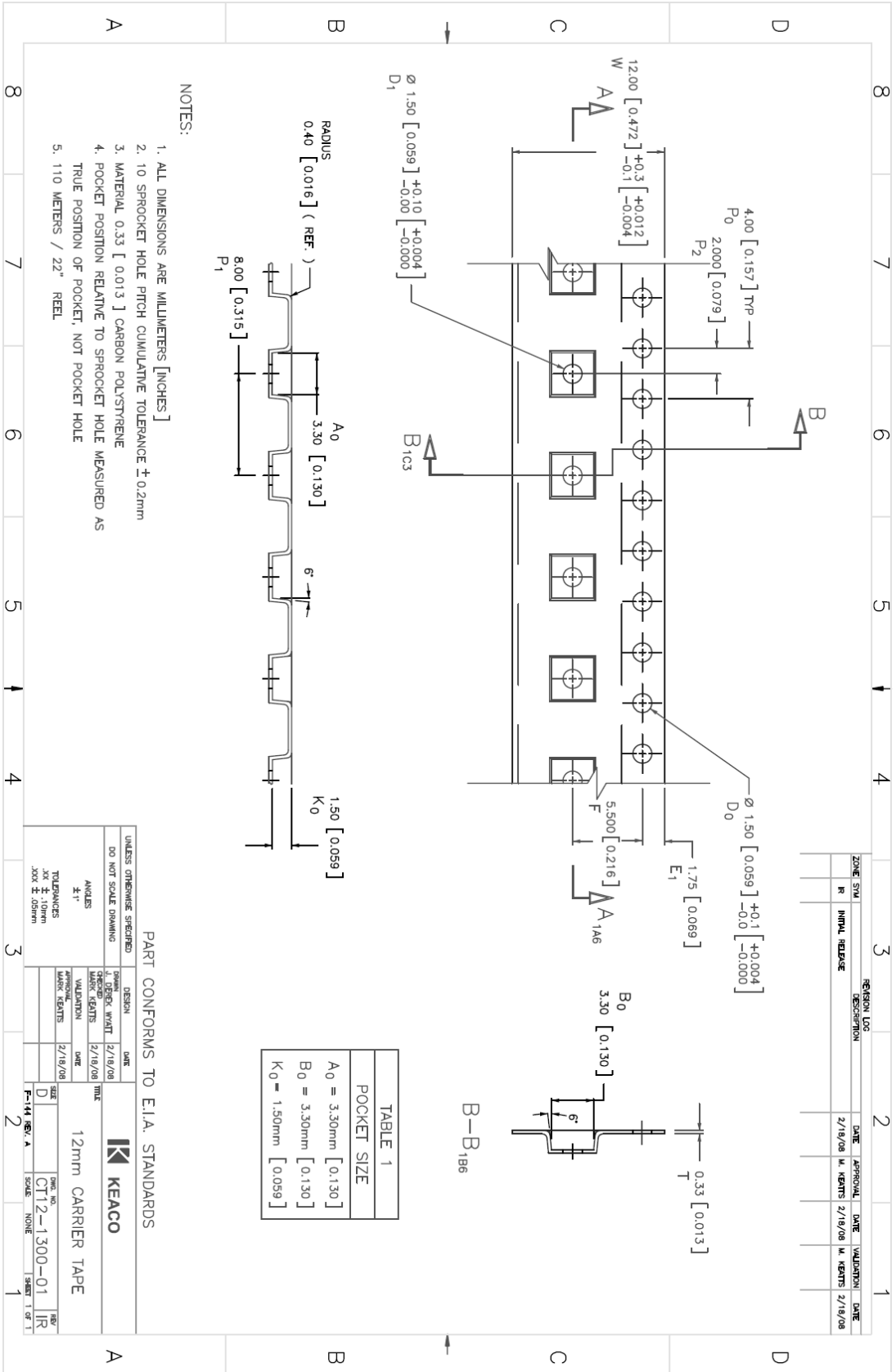


Figure 12. Dimensions of the reel

ZONE SWM		REGION LOG	
IR	INITIAL RELEASE	DATE	APPROVAL
		2/19/08	IN KEATS
		2/19/08	IN KEATS
		2/19/08	IN KEATS



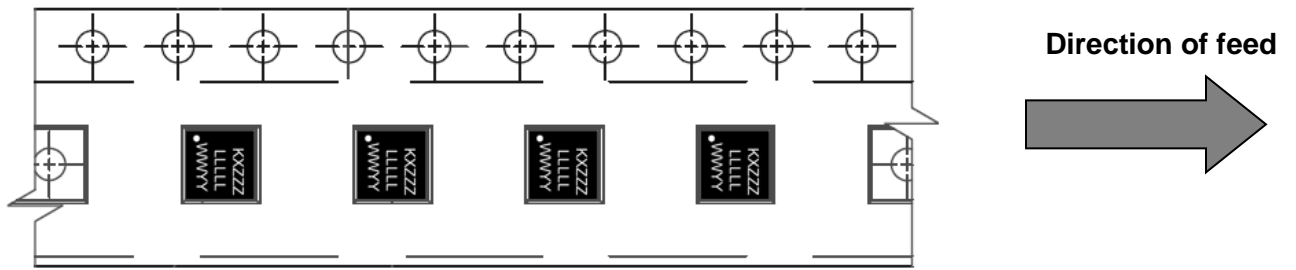


Figure 13. Orientation of the parts in the carrier tape and direction of feed

Revision History

Rev	Date	Description of Change
-	03-Jul-08	Initial release
2	29-Sep-11	Include 16 pin devices
3	3-Jan-12	Included 16 pin solder mask schematic
4	22-Mar-12	Added "Detail A" to illustrate metal lead dimension to Figures 2,3,4
5	12-June-14	Added Solder Pad Layer Dimensions
6	15-Oct-14	Added No solder on side of package recommendation.
7	07-May-15	Updated Solder Mask Defined feature drawings, removed 8 pin
8	10-July-15	Renamed the document
9	18-Jan-24	Replaced accelerometer with sensor
10	19-Mar-19	Update PCB Layout, Solder Stencil, and Via and Trace to current practices.

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