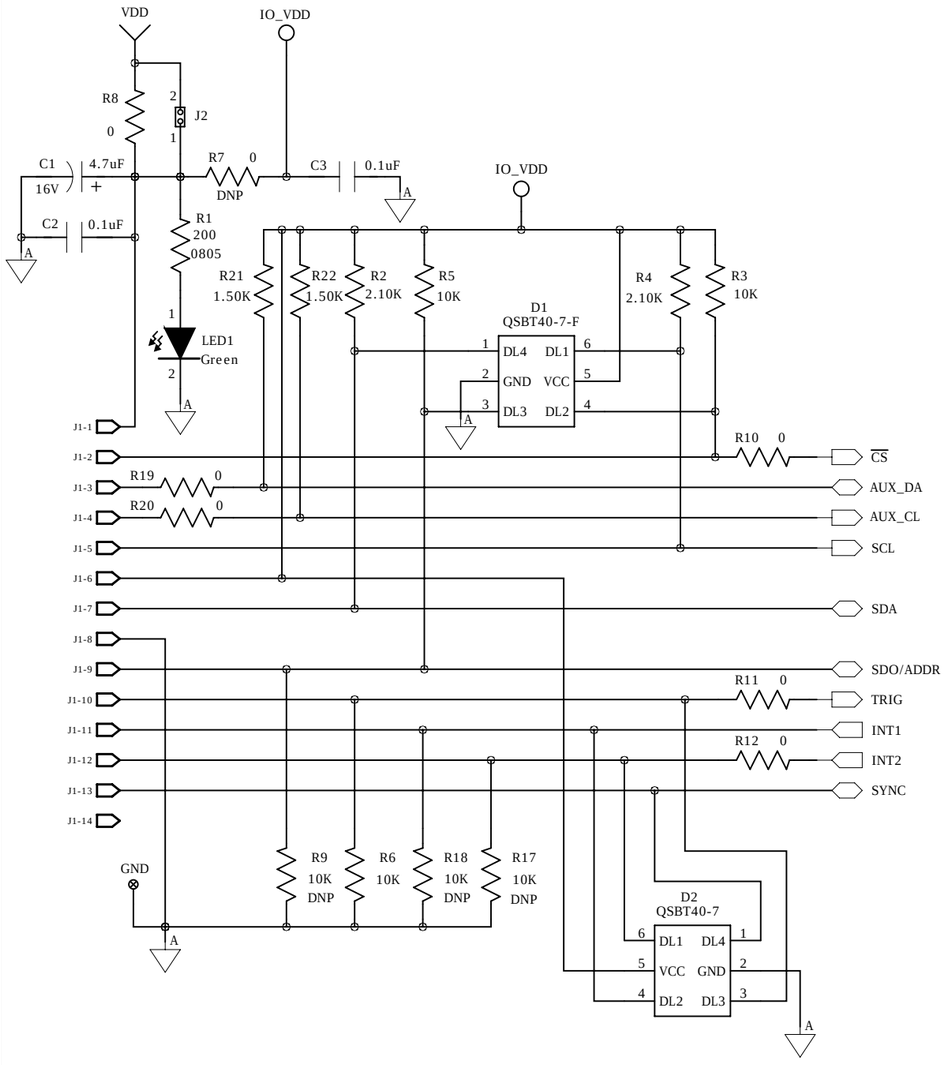
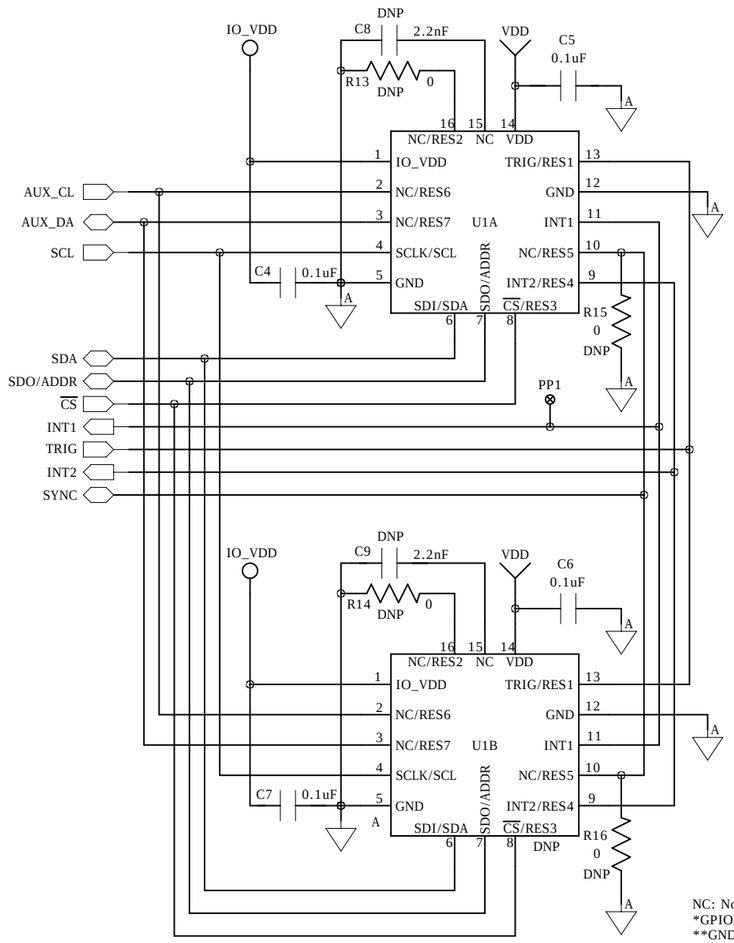


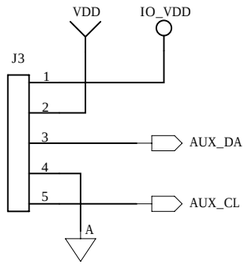


PIN	KX023 KX123 KX124 KX224	KMX62 KMX63	KMX64 KMX65		
1	IO_VDD	IO_VDD	IO_VDD		
2	NC	CAP	NC		
3	NC	GND**	NC		
4	SCLK/SCL	SCL	SCLK/SCL		
5	GND	GND**	GND^		
6	SDI/SDA	SDA	SDI/SDA		
7	SDO/ADDR	ADDR	SDO/ADDR		
8	nCS	NC	nCS		
9	INT2	GPIO2*	GPIO2*		
10	NC	NC	NC		
11	INT1	GPIO1*	GPIO1*		
12	GND	GND**	GND^		
13	TRIG	NC	NC		
14	VDD	VDD	VDD		
15	NC	NC	NC		
16	NC	NC	NC		

PIN	KXCJK	KXCNL	KXG03	KXG07	
1	IO_VDD	VIO	IO_VDD	IO_VDD	
2	NC	NC	AUX_CL	AUX_CL	
3	NC	NC	AUX_DA	AUX_DA	
4	SCL	SCL	SCLK/SCL	SCLK/SCL	
5	GND	GND	RESERVED	NC	
6	SDA	SDA	MOSI/SDA	MOSI/SDA	
7	ADDR	ADDR	MISO/ADDR	MISO/ADDR	
8	RSVD***	NC	nCS	nCS	
9	RSVD****	INT2	INT2	INT2	
10	RSVD****	NC	SYNC	NC	
11	INT	INT1	INT1	INT1	
12	GND	GND	GND	GND	
13	NC	NC	TRIG	SYNC_TRIG	
14	VDD	VDD	VDD	VDD	
15	NC	NC	CPOUT	NC	
16	NC	NC	RESERVED	NC	

NC: Not Connected internally. Can be connected to IO_VDD, GND, or left floating.
*GPIO1,GPIO2 pins 11, 9 cannot float when configured as an input on KMX62 and KMX63.
**GND pins 3, 5, 12 are internally tied together to GND on KMX62, KMX63, KMX64 and KMX65.
^GND pins 5 and 12 are internally tied together on KMX64 and KMX65.
***RSVD pin 8 must be connected to IO_VDD on KXTJK.
****RSVD pins 9, 10 are internally tied to GND. Connect to GND or leave floating on KXTJK.

NOTES:
1) All resistors are 1%, 1/10W, 0603 unless otherwise specified.
2) All capacitors are 0.1uF, 10%, 50V, 0603 unless otherwise specified.
3) U1:
   a) U1A: Sensor footprint.
   b) U1B: Socket footprint: Loranger, 03742 171 6218B.



DRAWN: J Zappala	DATED: 08/20/2018
CHECKED: A Chernyakov	DATED: 08/20/2018
QUALITY CONTROL:	DATED:
RELEASED:	DATED:

COMPANY: Kionix Inc.

TITLE: 3x3 LGA 16-Pin Evaluation Board

CODE:	SIZE:	DRAWING NO:	REV:
DWG988	B	KMAEDA001R01	H

SCALE: NONE SHEET: 1 of 2

REVISION RECORD				
DATE:	DRAWN BY:	DESCRIPTION:	CHECKED BY:	DATE:
12/08/2016	J Zappala	1) Initial release.		
12/09/2016	J Zappala	1) Add 10K pull-downs: J1-11, J1-12.		
		2) Add device pin notes.		
		3) Swap D1-3 and D1-4.		
		4) Add fiducials.		
02/08/2017	J Zappala	1) Add: D2; 2.2nF cap to U1A-15 and U1B-15; ATM and SYNC nets; J3, AUX_CL, and AUX_DA nets ,R19, and R20; KXG03 and KXG08 devices.		
02/09/2017	J Zappala	1) Add AUX_DA and AUX_CL to J1 and 1.5K pull-ups.		
		2) Remove ATM net.		
		3) Change J3-1 net name fro VDD_IO.		
		4) Update pin names in table.		
		5) Swap D1 connections.		
02/10/2017	J Zappala	1) Remove PP2 thru PP6. Move PP1 from U1A-15 to INT1.		
02/21/2017	J Zappala	1) Correct KX124-5 pin name from INT annd KX124-11 pin name from GND.		
12/21/2017	J Zappala	1) Add KMX63; update table and Note 4.		
08/20/2018	J Zappala	1) Add: KMX64, KMX65.		
		2) Delete: Note 4; I2C address.		
		3) Change: Note 3.		

MTHOLE1 MTHOLE150
MTHOLE2 MTHOLE150
MTHOLE3 MTHOLE150
MTHOLE4 MTHOLE150

FD1 FIDUCIAL_40MIL
FD2 FIDUCIAL_40MIL
FD3 FIDUCIAL_40MIL

LOGO1
Kionix Inc. LOGO

DRAWN: J Zappala	DATED: 08/20/2018		
CHECKED: A Chernyakov	DATED: 08/20/2018		
QUALITY CONTROL:	DATED:		
RELEASED:	DATED:		

COMPANY: Kionix Inc.

TITLE: 3x3 LGA 16-Pin Evaluation Board

CODE:	SIZE:	DRAWING NO:	REV:
DWG988	B	KMAEDA001R01	H

SCALE: NONE SHEET: 2 of 2