Table of Contents

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1. Introduction

The purpose of the application notes is to help customers to transition from KX222-1054 and KX224-1053 accelerometers to **KX134-1211** accelerometer.

2. Side-by-Side Comparison

The following are key side-by-side comparisons with the KX134-1211 accelerometers. Typical values are shown, unless otherwise indicated.

2.1. Features

		KX222 KX224	KX134-1211
Parameter	**Units**		
Low Power Mode		Yes	Yes
Self-test		Yes	Yes
Wake-up		Yes	Yes
Back-to-sleep		No	Yes
Freefall Detection		Yes	Yes
Tap, Double-Tap Detection		Yes	Yes
Tilt Orientation Detection		Yes	Yes
Pedometer		No	No
Advanced Data Path		No	Yes
User Configurable Full-Scale Range	g	±8/16/32	±8/16/32/64
Maximum Output Data Rate	Hz	25600	25600
Sample Buffer (FIFO)	Bytes	2048	512

Note: See *Key Functional Differences* section 4 for further details

2.2. Mechanical Specifications

			KX222 KX224	KX134-1211
Parameter		**Units**		
Operating Temperature Range		°C	-40 to 85	-40 to 105
Zero-g Offset		mg	±75	±75
Zero-g Offset Variation from RT over Temp.		mg/°C	±0.5	±0.5
Sensitivity	GSEL1=0, GSEL0=0 (±8g)	counts/g	4096	4096
	GSEL1=0, GSEL0=1 (±16g)		2048	2048
	GSEL1=1, GSEL0=0 (±32g)		1024	1024
	GSEL1=1, GSEL0=1 (±64g)			512
Sensitivity Variation from RT over Temp.		%/°C	0.01	0.01
Self-Test Output change on Activation*		g	0.5	0.5
Mechanical Signal Bandwidth (-3dB)		Hz	8000 (xy) 5100 (z)	8200 (x) 8500 (y) 5600 (z)
Non-Linearity		% of FS	0.6	0.6
Cross Axis Sensitivity		%	2	2
Noise (ODR = 50Hz, LPRO = 1)	RMS	mg	3.3	1.9
	Density	µg/√Hz	630	300

* See section 0 for details on Self-Test

2.3. Electrical Specifications

			KX222 KX224	KX134-1211
Parameter		**Units**		
Supply Voltage (VDD)		V	1.71–3.6	1.70–3.6
I/O Pads Supply Voltage (IO_VDD)	SPI, I^2C (Fast/Standard Mode)	V	1.7–3.6	1.2-3.6
	I^2C (High Speed mode)	V	1.7–3.6	1.7-3.6
Current Consumption (Typical)	High Resolution Mode (ODR=800Hz)	µA	145	148
	Low Power Mode (ODR=0.781Hz, 2 samples averaged)	µA	1.3	0.53
	Standby	µA	0.9	0.50
I^2C Communication Rate (max)		MHz	3.4	3.4
SPI Communication Rate (max)		MHz	10	10
Output Data Rate [ODR] (max)		kHz	25.6	25.6
I^2C Slave Address (7-bit)			0x1E/0x1F	0x1E/0x1F

2.4. Startup Time

ODR (Hz)	High Resolution / High Performance Mode (RES = 1)			Low Power Mode (RES = 0)	
	KX222 KX224	**KX134-1211 (FSTUP=0)**	**KX134-1211 (FSTUP=1)**	KX222 KX224	**KX134-1211 (FSTUP=N/A)**
0.781	1286.4	1283.0	1.9	1.4	1.9
1.563	643.9	642.2	1.9	1.4	1.9
3.125	322.6	322.0	1.9	1.4	1.9
6.25	162.1	161.7	1.9	1.4	1.9
12.5	81.7	81.7	1.9	1.4	1.9
25	41.5	41.6	1.9	1.4	1.9
50	21.5	21.6	1.9	1.4	1.9
100	11.4	11.6	1.9	1.4	1.9
200	6.4	6.6	1.9	1.4	1.9
400	3.9	4.1	1.9		1.9
800	2.7	2.8	2.8		
1600	2.0	2.2	2.2		
3200	1.7	1.9	1.9		
6400	1.6	1.7	1.7		
12800	1.5	1.7	1.7		
25600	1.4	1.6	1.6		

Table 1: Startup Time (msec) comparison

Notes:

1. Startup time is defined from setting PC1 bit in CNTL1 register to 1 until the valid outputs are available in output data registers.
2. Startup time varies with the power mode (RES bit in CNTL1 register) and the Output Data Rate (ODCNTL register).

2.5. POR Performance

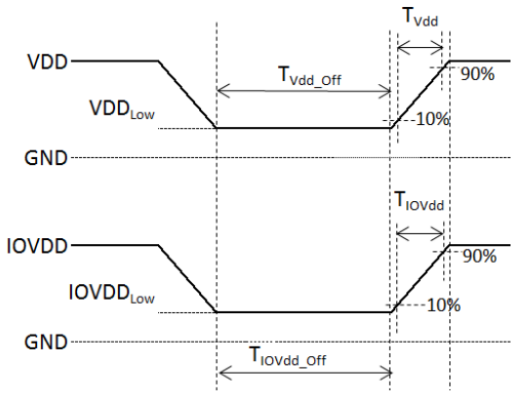


Figure 1: Power-On Reset Timing Diagram

Parameters	Units	KX222 KX224	KX134-1211
VDD rise time: T_{VDD}[1,2,3] (max)	ms	5	5
IO_VDD rise time: T_{IO_VDD}[1,2,3] (max)	ms	5	5
VDD off time: T_{VDD_OFF}[4,6] (min)	ms	20	20
IO_VDD off time: $T_{IO\_VDD\_OFF}$[4,6] (min)	ms	20	20
VDD low voltage: VDD_{Low}[4,6] (max)	mV	200	200
IO_VDD low voltage: IO_VDD_{Low}[4,6] (max)	mV	200	200
Software Reset Time[6] (max)	ms	2	2
Power Up Time[7] (typ / max)	ms	20 / 50	20 / 50

Table 2: POR Performance Comparison

Notes:

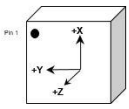
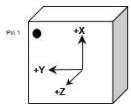
1. VDD and IO_VDD must always be monotonic ramps without ambiguous state.
2. T_{VDD} and T_{IO_VDD} rise from 10% to 90% of final value needs to be less than or equal the maximum duration specified in Table 2.
3. IO_VDD amplitude must remain ≤ VDD.
4. T_{VDD_OFF} and $T_{IO\_VDD\_OFF}$ are off times for VDD and IO_VDD voltage rails respectively. In order to prevent the accelerometer from entering an ambiguous state, both VDD and IO_VDD need to be pulled down to GND below the VDD_{Low} and IO_VDD_{Low} levels respectively for the duration of time at or above T_{VDD_OFF} and $T_{IO\_VDD\_OFF}$ respectively.
5. It is important the user determines the timing (T_{VDD_OFF}) and threshold (VDD_{LOW}) levels by evaluating the performance in the specific system for which the device will be incorporated.
6. Software Reset Time is defined as time it takes to perform a RAM reboot routine following the setting of SRST bit to 1 in the corresponding control register. The SRST bit will remain 1 until the RAM reboot routine is completed.
7. Power Up Time is defined as time from VDD and IO_VDD become valid to device boot completion.

2.6. Environmental

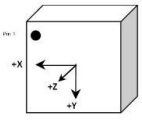
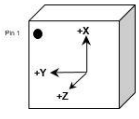
Parameter	Units	KX222 KX224	KX134-1211
Supply Voltage (VDD) | Absolute Limits	V	-0.5 to 3.60	-0.3 to 3.60
Operating Temperature Range	°C	-40 to 85	-40 to 105
Storage Temperature Range	°C	-55 to 150	-55 to 150
Mechanical Shock (powered and unpowered)	g	5000 for 0.5ms 10000 for 0.2ms	5000 for 0.5ms 10000 for 0.2ms
ESD (HBM)	V	2000	2000

2.7. Package Information

Comparison of KX222 with KX134-1211

Parameter	Units	KX222	KX134-1211
Sensing Axes (Accel)		XYZ 3-axis	XYZ 3-axis
Package Size	mm	2x2x0.9	2x2x0.9
Package Type		LGA	LGA
Pins		12	12
Axes Orientation			

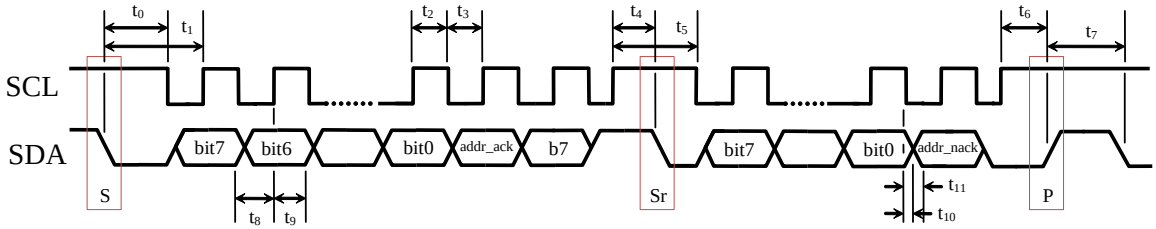
Comparison of KX224 sensor with KX134-1211

Parameter	Units	KX224	KX134-1211
Sensing Axes (Accel)		XYZ 3-axis	XYZ 3-axis
Package Size	mm	3x3x0.9	2x2x0.9
Package Type		LGA	LGA
Pins		16	12
Axes Orientation			

2.8. Digital Interface

2.8.1. I²C Interface

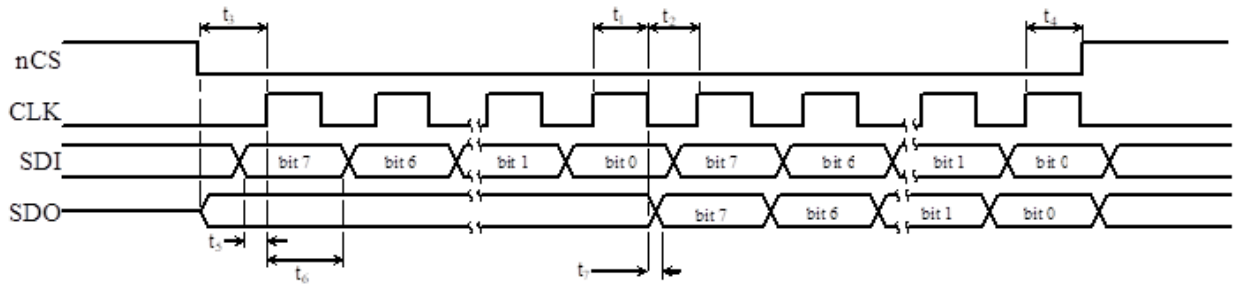
The I²C Interface timing for all products is the same. Also, the 7-bit I²C Slave Address for all parts can be either 0x1E or 0x1F, as determined by the physical connection of the ADDR pin.



Number	Description	MIN	MAX	Units
t_0	SDA LOW to SCL LOW transition (Start event)	50	-	ns
t_1	SDA LOW to first SCL rising edge	100	-	ns
t_2	SCL pulse width: HIGH	100	-	ns
t_3	SCL pulse width: LOW	100	-	ns
t_4	SCL HIGH before SDA falling edge (Start Repeated)	50	-	ns
t_5	SCL pulse width: HIGH during a S/Sr/P event	100	-	ns
t_6	SCL HIGH before SDA rising edge (Stop)	50	-	ns
t_7	SDA pulse width: HIGH	25	-	ns
t_8	SDA valid to SCL rising edge	50	-	ns
t_9	SCL rising edge to SDA invalid	50	-	ns
t_{10}	SCL falling edge to SDA valid (when slave is transmitting)	-	100	ns
t_{11}	SCL falling edge to SDA invalid (when slave is	0	-	ns
Note	Recommended I²C CLK	2.5	-	µs

2.8.2. SPI Interface

2.8.2.1. 4-Wire SPI Interface Timing

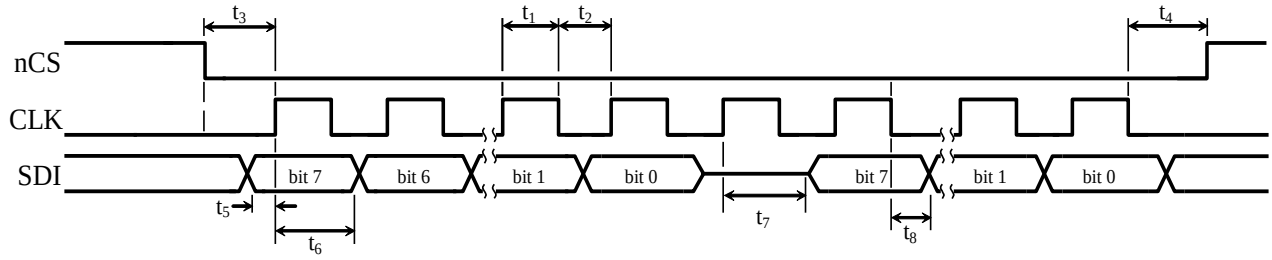


The min specification for several parameter vary between KX134-1211 and other products as shown in the Table 3.

		KX222 KX224	**KX134-1211**	KX222 KX224 **KX134-1211**	
Number	**Description**	**MIN**		**MAX**	**Units**
t_1	CLK pulse width: HIGH	40	45		ns
t_2	CLK pulse width: LOW	40	45		ns
t_3	nCS LOW to first CLK rising edge	20	20		ns
t_4	nCS LOW after the final CLK rising edge to nCS HIGH	30	20		ns
t_5	SDI valid to CLK rising edge	10	10		ns
t_6	CLK rising edge to SDI invalid	10	10		ns
t_7	CLK falling edge to SDO valid			35	ns

Table 3: 4-Wire SPI Interface Timing

2.8.2.2. 3-Wire SPI Interface Timing



The min specification for several parameter vary between KX134-1211 and other products as shown in the Table 4.

		KX222 KX224	**KX134-1211**	KX222 KX224 **KX134-1211**	
Number	**Description**	**MIN**		**MAX**	**Units**
t_1	CLK pulse width: HIGH	40	45		ns
t_2	CLK pulse width: LOW	40	45		ns
t_3	nCS LOW to first CLK rising edge	20	20		ns
t_4	nCS LOW after the final CLK rising edge to nCS HIGH	20	20		ns
t_5	SDI valid to CLK rising edge	10	10		ns
t_6	CLK rising edge to SDI input valid	10	10		ns
t_7	CLK extra clock cycle rising edge to SDI output becomes valid	-	-	-	ns
t_8	CLK falling edge to SDI output becomes valid			35	ns

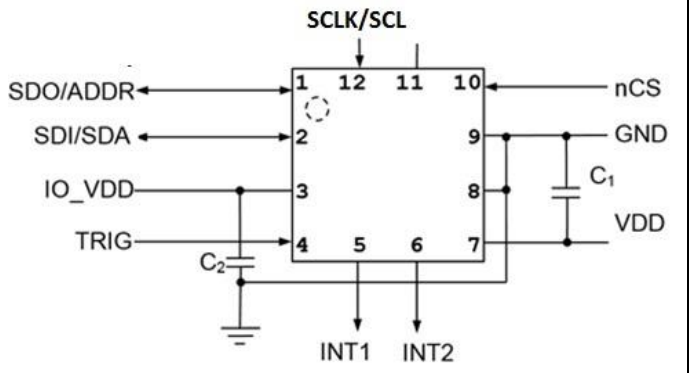
Table 4: 3-Wire SPI Interface Timing

2.9. Pin Compatibility / Application Schematic

2.9.1. KX222 vs. KX134-1211

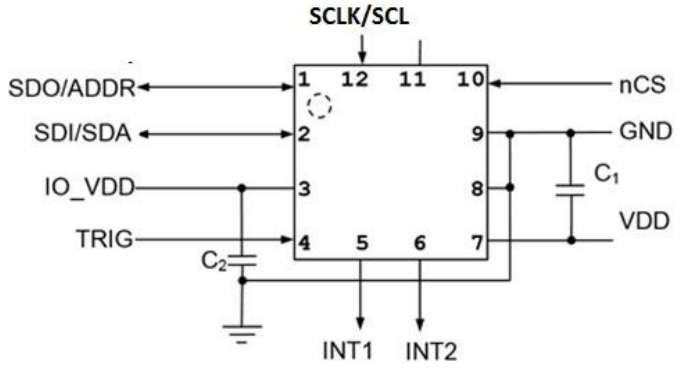
The KX222 accelerometer can be easily replaced by the KX134-1211 accelerometer for either an I²C or SPI interface application. From a hardware perspective, all these sensors have an identical pad/pin layouts and identical pin functionality.

KX222



Pin	Name	Description
1	SDO/ADDR	Serial Data Out pin during 4-wire SPI communication and part of the device address during I2C communication. Do not leave floating.
2	SDI/SDA	SPI Data input / I2C Serial Data
3	IO_VDD	The power supply input for the digital communication bus. Optionally decouple this pin to ground with a 0.1µF ceramic capacitor.
4	TRIG	Trigger pin for FIFO buffer control. Connect to GND when not using external trigger option.
5	INT1	Physical Interrupt 1 (Push-Pull). The pin is in High-Z state during POR and is driven LOW following POR. Leave floating if not used.
6	INT2	Physical Interrupt 2 (Push-Pull). The pin is in High-Z state during POR and is driven LOW following POR. Leave floating if not used.
7	VDD	The power supply input. Decouple this pin to ground with a 0.1µF ceramic capacitor.
8	GND	Ground
9	GND	Ground
10	nCS	Chip Select (active LOW) for SPI communication. Connect to IO_VDD for I2C communication. Do not leave floating.
11	NC	Not Internally Connected. Can be connected to VDD, IO_VDD, GND or leave floating.
12	SCLK/SCL	SPI and I2C Serial Clock

KX134-1211

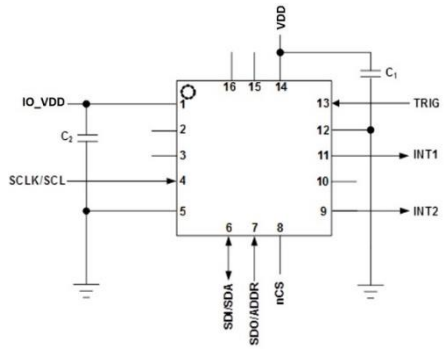


Pin	Name	Description
1	SDO/ADDR	Serial Data Out pin during 4-wire SPI communication and part of the device address during I2C communication. Do not leave floating.
2	SDI/SDA	SPI Data input / I2C Serial Data
3	IO_VDD	The power supply input for the digital communication bus. Optionally decouple this pin to ground with a 0.1µF ceramic capacitor.
4	TRIG	Trigger pin for FIFO buffer control. Connect to GND when not using external trigger option.
5	INT1	Physical Interrupt 1 (Push-Pull). The pin is in High-Z state during POR and is driven LOW following POR. Leave floating if not used.
6	INT2	Physical Interrupt 2 (Push-Pull). The pin is in High-Z state during POR and is driven LOW following POR. Leave floating if not used.
7	VDD	The power supply input. Decouple this pin to ground with a 0.1µF ceramic capacitor.
8	GND	Ground
9	GND	Ground
10	nCS	Chip Select (active LOW) for SPI communication. Connect to IO_VDD for I2C communication. Do not leave floating.
11	NC	Not Internally Connected. Can be connected to VDD, IO_VDD, GND or leave floating.
12	SCLK/SCL	SPI and I2C Serial Clock

2.9.2. KX224 vs. KX134-1211

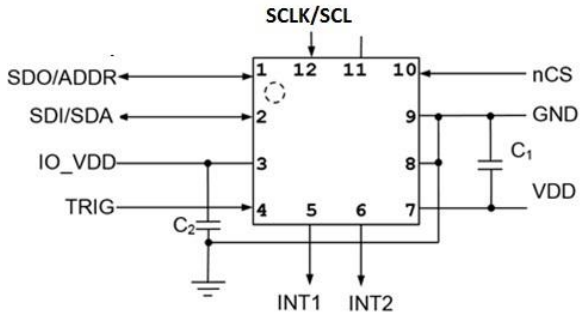
The KX224 accelerometer come in a 3 x 3 x 0.9 mm LGA 16-pin package, which is different from 2 x 2 x 0.9 mm LGA 12-pin package for the KX134-1211. Thus, the KX134-1211 is **not** a direct drop-in replacement for the KX224. However, the functionality of identically called pins is the same between sensors.

KX224



Pin	Name	Description
1	IO_VDD	The power supply input for the digital communication bus. Optionally decouple this pin to ground with a 0.1µF ceramic capacitor.
2	NC	Not Internally Connected. Can be connected to VDD, IO_VDD, GND or leave floating.
3	NC	Not Internally Connected. Can be connected to VDD, IO_VDD, GND or leave floating.
4	SCLK/SCL	SPI and I2C Serial Clock
5	GND	Ground
6	SDI/SDA	SPI Data input / I2C Serial Data
7	SDO/ADDR	Serial Data Out pin during 4-wire SPI communication and part of the device address during I2C communication. Do not leave floating.
8	nCS	Chip Select (active LOW) for SPI communication. Connect to IO_VDD for I2C communication. Do not leave floating.
9	INT2	Physical Interrupt 2 (Push-Pull). The pin is in High-Z state during POR and is driven LOW following POR. Leave floating if not used.
10	NC	Not Internally Connected. Can be connected to VDD, IO_VDD, GND or leave floating.
11	INT1	Physical Interrupt 1 (Push-Pull). The pin is in High-Z state during POR and is driven LOW following POR. Leave floating if not used.
12	GND	Ground
13	TRIG	Trigger pin for FIFO buffer control. Connect to GND when not using external trigger option.
14	VDD	The power supply input. Decouple this pin to ground with a 0.1µF ceramic capacitor.
15	NC	Not Internally Connected. Can be connected to VDD, IO_VDD, GND or leave floating.
16	NC	Not Internally Connected. Can be connected to VDD, IO_VDD, GND or leave floating.

KX134-1211



Pin	Name	Description
1	SDO/ADDR	Serial Data Out pin during 4-wire SPI communication and part of the device address during I2C communication. Do not leave floating.
2	SDI/SDA	SPI Data input / I2C Serial Data
3	IO_VDD	The power supply input for the digital communication bus. Optionally decouple this pin to ground with a 0.1µF ceramic capacitor.
4	TRIG	Trigger pin for FIFO buffer control. Connect to GND when not using external trigger option.
5	INT1	Physical Interrupt 1 (Push-Pull). The pin is in High-Z state during POR and is driven LOW following POR. Leave floating if not used.
6	INT2	Physical Interrupt 2 (Push-Pull). The pin is in High-Z state during POR and is driven LOW following POR. Leave floating if not used.
7	VDD	The power supply input. Decouple this pin to ground with a 0.1µF ceramic capacitor.
8	GND	Ground
9	GND	Ground
10	nCS	Chip Select (active LOW) for SPI communication. Connect to IO_VDD for I2C communication. Do not leave floating.
11	NC	Not Internally Connected. Can be connected to VDD, IO_VDD, GND or leave floating.
12	SCLK/SCL	SPI and I2C Serial Clock

2.10. **Embedded Registers**

The Table 5 shows the side-by-side comparison of the embedded registers between the sensors. Some of the most commonly used registers are highlighted for better visualization. Note, that registers with similar names may have different bit functions. See section 4 for details.

Addr (HEX)	KX222 KX224	KX134-1211
0	XHP_L	MAN_ID
1	XHP_H	PART_ID
2	YHP_L	XADP_L
3	YHP_H	XADP_H
4	ZHP_L	YADP_L
5	ZHP_H	YADP_H
6	XOUT_L	ZADP_L
7	XOUT_H	ZADP_H
8	YOUT_L	XOUT_L
9	YOUT_H	XOUT_H
0A	ZOUT_L	YOUT_L
0B	ZOUT_H	YOUT_H
0C	COTR	ZOUT_L
0D	Kionix Reserved	ZOUT_H
0E	Kionix Reserved	Kionix Reserved
0F	WHO_AM_I	Kionix Reserved
10	TSCP	Kionix Reserved
11	TSPP	Kionix Reserved
12	INS1	COTR
13	INS2	WHO_AM_I
14	INS3	TSCP
15	STAT	TSPP
16	Kionix Reserved	INS1
17	INT_REL	INS2
18	CNTL1	INS3
19	CNTL2	STATUS_REG
1A	CNTL3	INT_REL
1B	ODCNTL	CNTL1
1C	INC1	CNTL2
1D	INC2	CNTL3
1E	INC3	CNTL4
1F	INC4	CNTL5
20	INC5	CNTL6
21	INC6	ODCNTL
22	TILT_TIMER	INC1

23	WUFC	INC2
24	TDTRC	INC3
25	TDTC	INC4
26	TTH	INC5
27	TTL	INC6
28	FTD	Kionix Reserved
29	STD	TILT_TIMER
2A	TLT	TDTRC
2B	TWS	TDTC
2C	FFTH	TTH
2D	FFC	TTL
2E	FFCNTL	FTD
2F	Kionix Reserved	STD
30	ATH	TLT
31	Kionix Reserved	TWS
32	TILT_ANGLE_LL	FFTH
33	TILT_ANGLE_HL	FFC
34	HYST_SET	FFCNTL
35	LP_CNTL	Kionix Reserved
36	Kionix Reserved	TILT_ANGLE_LL
37	Kionix Reserved	TILT_ANGLE_HL
38	Kionix Reserved	HYST_SET
39	Kionix Reserved	LP_CNTL1
3A	BUF_CNTL1	LP_CNTL2
3B	BUF_CNTL2	Kionix Reserved
3C	BUF_STATUS_1	Kionix Reserved
3D	BUF_STATUS_2	Kionix Reserved
3E	BUF_CLEAR	Kionix Reserved
3F	BUF_READ	Kionix Reserved
40	Kionix Reserved	Kionix Reserved
41	Kionix Reserved	Kionix Reserved
42	Kionix Reserved	Kionix Reserved
43	Kionix Reserved	Kionix Reserved
44	Kionix Reserved	Kionix Reserved
45	Kionix Reserved	Kionix Reserved
46	Kionix Reserved	Kionix Reserved
47	Kionix Reserved	Kionix Reserved
48	Kionix Reserved	Kionix Reserved
49	Kionix Reserved	WUFTH
4A	Kionix Reserved	BTSWUFTH
4B	Kionix Reserved	BTSTH
4C	Kionix Reserved	BTSC
4D	Kionix Reserved	WUFC

4E-4F	Kionix Reserved	Kionix Reserved
5A	Kionix Reserved	Kionix Reserved
5B	Kionix Reserved	Kionix Reserved
5C	Kionix Reserved	Kionix Reserved
5D	Kionix Reserved	SELF_TEST
5E	Kionix Reserved	BUF_CNTL1
5F	Kionix Reserved	BUF_CNTL2
60	SELF_TEST	BUF_STATUS_1
61	Kionix Reserved	BUF_STATUS_2
62	Kionix Reserved	BUF_CLEAR
63	Kionix Reserved	BUF_READ
64-76	Kionix Reserved	ADP_CNTL(1-19)
77-7F	Kionix Reserved	Kionix Reserved

Table 5: Register Map Comparison

3. Key Functional Similarities

The KX222/KX224 and KX134-1211 accelerometer outputs are all 16-bit. The sensitivity is the same and thus acceleration conversation is the same from counts to 'g'.

The Free fall, Tap/Double-Tap, and Tilt engines operate the same way, with the same register settings. For information regarding Wake-Up and Back-to-Sleep engine, see section 4.5 for details.

4. Key Functional Differences

4.1. Advanced Data Path

The Advanced Data Path (ADP) is a unique feature of the KX134-1211 accelerometer that provides an additional way to process the raw data captured by the accelerometer via a highly configurable 3-stage solution. The first stage consists of a 2nd order low-pass filter with adjustable cut-off. The second stage can be configured as either 1st order low-pass filter or 1st order high-pass filter with adjustable cut-off. The 3rd stage is the RMS engine with configurable averaging setting. Each stage of the ADP can be bypassed, and the data is processed at the Output Data Rate set independently of the main/standard data path. The post-processed data from the Advanced Data Path can be routed to the dedicated output data registers or buffered. It also can be routed to the Wake-Up / Back-to-Sleep engine. For additional details on the Advanced Data Path, see AN109 Introduction to Advanced Data Path application note.

4.2. High-Pass Filter Outputs

The KX134-1211 accelerometer does not support high-pass filter outputs of the raw data, which were the difference between the current and present sample and available when wake-up engine was enabled.

4.3. Free fall Engine

The free fall engine in the KX134-1211 accelerometer can detect the event of the free fall and operates the same way as in KX222/KX224 accelerometers.

4.4. Output Data Rates (ODR)

The KX134-1211 accelerometer adds support for 400Hz in Low Power Mode (Table 6).

ODR (Hz)	Low Power Mode		High Resolution / High Performance Mode	
	KX222 KX224	KX134-1211	KX222 KX224	KX134-1211
0.781				
1.563				
3.125				
6.25				
12.5				
25				
50				
100				
200				
400				
800				
1600				
3200				
6400				
12800				
25600				

Table 6: Maximum Supported Output Data Rate (ODR) vs. Power Mode

ODR is supported in Low Power mode
ODR is not supported in the indicated power mode
ODR is supported in High Performance / High Resolution modes

The definition of the OSA<3:0> bit settings in ODCNTL registers varies between different products as shown in Table 7 (the highlighted values is the default / factory programmed value).

				KX222 KX224	KX134-1211
OSA3	**OSA2**	**OSA1**	**OSA0**	**ODR (Hz)**	**ODR (Hz)**
0	0	0	0	12.5	0.781
0	0	0	1	25	1.563
0	0	1	0	50	3.125
0	0	1	1	100	6.25
0	1	0	0	200	12.5
0	1	0	1	400	25
0	1	1	0	800	50
0	1	1	1	1600	100
1	0	0	0	0.781	200
1	0	0	1	1.563	400
1	0	1	0	3.125	800
1	0	1	1	6.25	1600
1	1	0	0	3200	3200
1	1	0	1	6400	6400
1	1	1	0	12800	12800
1	1	1	1	25600	25600

Table 7: OSA<3:0> bit settings definition

The definition of the OTDT<2:0> bits in CNTL3 registers has been updated as shown in Table 8 (the highlighted values is the default / factory programmed value).

			KX222 KX224	KX134-1211
OTDT2	**OTDT1**	**OTDT0**	**ODR (Hz)**	**ODR (Hz)**
0	0	0	50	12.5
0	0	1	100	25
0	1	0	200	50
0	1	1	400	100
1	0	0	12.5	200
1	0	1	25	400
1	1	0	800	800
1	1	1	1600	1600

Table 8: OTDT<3:0> bit settings definition

4.5. Wake-up and Back-to-Sleep Engine

4.5.1. Back-to-Sleep Engine

The KX134-1211 accelerometer offers a back-to-sleep engine that can be configured independently of the Wake-Up engine. The Back-to-Sleep engine was not supported in KX222 or KX224 sensors.

4.5.2. Wake-up / Back-to-Sleep Resolution / Threshold Value

The KX134-1211 accelerometer offers a higher resolution threshold setting unlike the KX222 or KX224 accelerometers, resulting in more versatile detection.

4.5.2.1. KX222, KX224

The thresholds for the Wake-up engine in KX222/KX224 accelerometers is set by ATH<7:0> bits in Activity Threshold (ATH) register. The value is compared to the top **8 bits** of the accelerometer 32g output (regardless of GSEL<1:0> setting in CNTL1 register). The setting is calculated both on positive and negative directions of the motion. This results in a threshold of **4 counts/g** or resolution of **250 mg/count** per Equation 1.

$$2^8 \text{ counts} / (\pm 32 \text{ g}) = 256 \text{ counts} / 64 \text{ g} = 4 \text{ counts/g or } 250 \text{ mg/count}$$

Equation 1: Wake-Up / Back-to-Sleep Resolution Calculations

The factory default value for the Wake-up and Back-to-Sleep engines is set to 2 counts or **0.5g**.

4.5.2.2. KX134-1211

The thresholds for the Wake-up and Back-to-Sleep engines in KX126/KX127 as well as KX134-1211 accelerometers are set by WUFTH<10:0> and BTSTH<10:0> bits in WUFTH, BTSWUFTH, BTSTH registers. The values in these registers are compared to the top **11 bits** of the accelerometer 32g output (regardless of GSEL<1:0> setting in CNTL1 register) absolute value. This results in a threshold of **64 counts/g** or resolution of **15.6 mg/count** per Equation 2.

$$2^{11} \text{ counts} / 32 \text{ g} = 2048 \text{ counts} / 32 \text{ g} = 64 \text{ counts/g or } 15.6 \text{ mg/count}$$

Equation 2: Wake-Up / Back-to-Sleep Resolution Calculations

The factory default value for the Wake-up and Back-to-Sleep engines is set to 32 counts or **0.5g**.

4.5.3. Pulse Reject Mode

In KX134-1211, the Wake-Up and Back-to-Sleep digital engines can be configured to ignore pulse-like motion using PR_MODE bit in CNTL4 register. See KX134-1211 Technical Reference Manual for additional information on Pulse Reject Mode.

4.5.1. Integration with Advanced Data Path

In KX134-1211, the output from the Advanced Data Path can be routed to the Wake-Up / Back-to-Sleep engines using a series of internal MUXes to be used instead of the standard accelerometer outputs. See KX134-1211 Technical Reference Manual for additional information on Advanced Data Path.

4.6. WHO_AM_I Register Value

WHO_AM_I Register will report a different value to discern between Kionix's sensors (Table 9).

Part	Register Name	Register Address	Register Value
KX222	WHO_AM_I	0x0F	0x2C
KX224			0x2B
KX134-1211		0x13	0x3D

Table 9: Factory Programmed WHO_AM_I Register Value

4.7. Advance Low Power Control Setting (LP_CNTL2)

KX134-1211 accelerometer offers an advanced low power control that reduces the power consumption even further in Low Power and Standby modes. The setting can only be used with Wake-up / Back-to-Sleep engine. The settings should not be used when other digital engines are used. See KX134-1211 Technical Reference Manual for additional information on LP_CNTL2 register setting.

4.8. IIR_BYPASS

KX134-1211 does not support bypass mode for low-pass IIR filter.

4.9. Buffer Operation

The Table 10 shows the difference in implementation of the buffer functionality between different products.

Parameters	Units	KX222 KX224	KX134-1211
Buffer Size	Bytes	2048	512
Full buffer capacity (8-bit samples)	Samples	681	171
Full buffer capacity (16-bit samples)	Sample	340	86
Buffer Threshold number of bit (SMP_TH)[1]	Bits	10 SMP_TH <9:0>	8 SMP_TH <7:0>
Buffer Sample Level number of bits (SMP_LVL)[2]	Bits	11 SMP_LVL<10:0>	10 SMP_LVL<9:0>
Buffer Auto Cleared[3]		(A), (B), (C), (D)	(A), (B), (C), (D)
Buffer Modes Supported		FIFO STREAM TRIGGER FILO	FIFO STREAM TRIGGER

Table 10: Buffer Size Comparison

Notes:

1. Bits SMP_TH<7:0> are located in BUF_CNTL1 register. Bits SMP_TH<9:8> are located in BUF_CNTL2 register.

2. Bits SMP_LVL<7:0> are located in BUF_STATUS_1 register. Bits SMP_LVL<11:8> are located in BUF_STATUS_2 register.

3. The buffer is auto cleared by one of the following actions:
   (A) – Buffer is read out with reading from BUF_READ register
   (B) – Buffer is cleared with writing to BUF_CLEAR register
   (C) – Buffer is disabled (setting BUFE bit to 0 in BUF_CNTL2 register)
   (D) – Accelerometer is disabled (PC1 bit is set to 0 in CNTL1 register)

4.10. Self-Test Testing Functionality

Generally, the self-test operation is performed by (1) setting the polarity bit STPOL to a predetermined value, (2) writing 0xCA to MEMS self-test enable register SELF_TEST, and (3) enabling the accelerometer by setting PC1 bit to 1 in CNTL1 register. The selt-test response is then calculated between the self-test ON and self-test OFF output response for each axes and the response should be compared to the products specifications to determine if the MEMS response is within the specified range (see SELF_TEST register description in the product specifications / technical reference manual for details). Please reference Table for details on how to set the STPOL value for testing X, Y, Z axes for each product.

Parameters	KX222 KX224	KX134-1211
STPOL bit value (X - axis)	1	0
STPOL bit value (Y – axis)	1	0
STPOL bit value (Z – axis)	1	0

Table 11: STPOL polarity bit value required to perform the test