

Introduction

The purpose of this application note is to illustrate how the Kionix KX124 accelerometer can replace an existing Kionix KX023 accelerometer.

Pin Compatibility

The KX023 accelerometer can be easily replaced by a KX124 accelerometer for either an I2C or SPI interface application. From a hardware perspective, the KX124 is a drop-in replacement for the KX023. Both parts are 3x3x0.9mm in size and have identical pad/pin layouts.

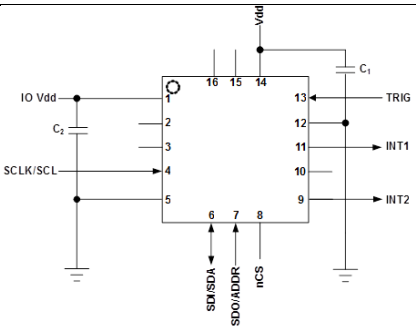
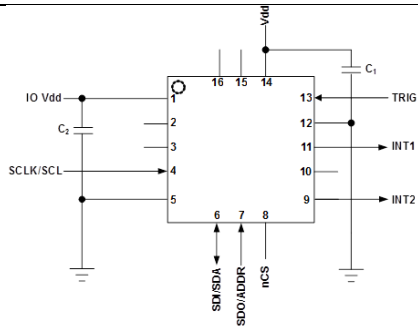
KX023			KX124		
					
Pin	Name	Description	Pin	Name	Description
1	IO_VDD	The power supply input for the digital communication bus. Optionally decouple this pin to ground with a 0.1uF ceramic capacitor.	1	IO_VDD	The power supply input for the digital communication bus. Optionally decouple this pin to ground with a 0.1uF ceramic capacitor.
2	NC	Not Internally Connected – Can be connected to VDD, IO_VDD, GND or leave floating	2	NC	Not Internally Connected – Can be connected to VDD, IO_VDD, GND or leave floating
3	NC	Not Internally Connected – Can be connected to VDD, IO_VDD, GND or leave floating	3	NC	Not Internally Connected – Can be connected to VDD, IO_VDD, GND or leave floating
4	SCLK/SCL	SPI and I ² C Serial Clock	4	SCLK/SCL	SPI and I ² C Serial Clock
5	GND	Ground	5	GND	Ground
6	SDI/SDA	SPI Data input / I2C Serial Data	6	SDI/SDA	SPI Data input / I2C Serial Data
7	SDO/ADDR	Serial Data Out pin during 4 wire SPI communication and part of the device address during I2C communication.	7	SDO/ADDR	Serial Data Out pin during 4 wire SPI communication and part of the device address during I2C communication.
8	nCS	SPI enable / I2C mode select. Connect to GND for SPI enabled, I2C communication disabled. Connect to IO_VDD for SPI disabled, I2C communication enabled. Do not leave floating.	8	nCS	SPI enable / I2C mode select. Connect to GND for SPI enabled, I2C communication disabled. Connect to IO_VDD for SPI disabled, I2C communication enabled. Do not leave floating.
9	INT2	Physical Interrupt 2. Leave floating if not used.	9	INT2	Physical Interrupt 2. Leave floating if not used.
10	NC	Not Internally Connected – Can be connected to VDD, IO_VDD, GND or leave floating	10	NC	Not Internally Connected – Can be connected to VDD, IO_VDD, GND or leave floating
11	INT1	Physical Interrupt 1. Leave floating if not used.0	11	INT1	Physical Interrupt 1. Leave floating if not used.0
12	GND	Ground	12	GND	Ground
13	TRIG	Trigger pin for FIFO buffer control – Connect to GND when not using external trigger option.	13	TRIG	Trigger pin for FIFO buffer control – Connect to GND when not using external trigger option.
14	VDD	The power supply input. Decouple this pin to ground with a 0.1uF ceramic capacitor.	14	VDD	The power supply input. Decouple this pin to ground with a 0.1uF ceramic capacitor.
15	NC	Not Internally Connected – Can be connected to VDD, IO_VDD, GND or leave floating	15	NC	Not Internally Connected – Can be connected to VDD, IO_VDD, GND or leave floating
16	NC	Not Internally Connected – Can be connected to VDD, IO_VDD, GND or leave floating	16	NC	Not Internally Connected – Can be connected to VDD, IO_VDD, GND or leave floating

Figure 1: Pin Description for KX023 and KX124

Key Similarities

- KX124 and KX023 accelerometer outputs are both 16-bit.
- KX124 and KX023 share identical register mappings, with the exception that the KX124 has more registers / bits that were previously reserved in the KX023 to support additional features. Any software register control currently written for the KX023, will work seamlessly with the KX124. Interrupt control and configurations registers are identical (mapping).
- KX124 and KX023 also share the same embedded application engines. Any software currently controlling the KX023 application engines, will inherently work for the KX124. This means no changes to threshold and/or timer settings will be required.

Key Differences

- New Features:
 - The KX023 is a first-generation design of a high performance, feature-rich accelerometer. The KX124 is a second-generation design that additionally offers:
 - Free-fall Engine: An embedded application engine that offers notification when the accelerometer senses a free-fall event.
 - 2048-byte Sample Buffer: This buffer is eight (8) times larger than the KX023's
 - Higher Sample Rates (up to 25.6kHz)
 - KX023 offers ODR settings of 0.781Hz, 1.563Hz, 3.125Hz, 6.25Hz, 12.5Hz, 25Hz, 50Hz, 100Hz, 200Hz, 400Hz, 800Hz, and 1600Hz.
 - KX124 offers the same ODR settings as KX023, but additionally offers 3200Hz, 6400Hz, 12800Hz, and 25600Hz.
- Buffer Operation:
 - Buffer Size
 - KX023 buffer size is 256 bytes – up to 84 (8-bit) and 41 (16-bit) samples can be stored.
 - KX124 buffer size is 2048 bytes – up to 681 (8-bit) and 340 (16-bit) samples can be stored.
 - Buffer Auto-Clear
 - KX023 doesn't clear the content of the buffer after buffer is disabled. The content of the buffer will remain the same until (1) the data is read out or (2) the buffer is cleared.
 - KX124 clears the content of the buffer after buffer is disabled. The content of the buffer will remain the same until (1) the data is read out or (2) the buffer is cleared or (3) the buffer is disabled.

- **Sample Threshold (SMP_TH)** – controls the number of sample that will trigger a watermark interrupt or will be saved prior to a trigger event
 - Sample threshold bits (SMP_TH) have been expanded to 9 bits to support the larger buffer
 - Like the KX023, bits SMP_TH[7:0] still exist in BUF_CNTL1
 - In the KX124, the expanded bits SMP_TH[9:8] can be found in BUF_CNTL2[3:2]

BUF_CNTL1

Read/write control register that controls the buffer sample threshold. Note that to properly change the value of this register, the PC1 bit in CNTL1 must first be set to "0".

R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	
-	SMP_TH6	SMP_TH5	SMP_TH4	SMP_TH3	SMP_TH2	SMP_TH1	SMP_TH0	Reset Value
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	00000000
I ² C Address: 0x3Ah								

SMP_TH[6:0] Sample Threshold: determines the number of samples that will trigger a watermark interrupt or will be saved prior to a trigger event. When BUF_RES=1, the maximum number of samples is 41; when BUF_RES=0, the maximum number of samples is 84.

Figure 2: KX023 SMP_TH Register/Bit Mapping

BUF_CNTL1

Read/write control register that controls the buffer sample threshold. Note that to properly change the value of this register, the PC1 bit in CNTL1 must first be set to "0".

R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	
SMP_TH7	SMP_TH6	SMP_TH5	SMP_TH4	SMP_TH3	SMP_TH2	SMP_TH1	SMP_TH0	Reset Value
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	00000000
I ² C Address: 0x3Ah								

BUF_CNTL2

Read/write control register that controls sample buffer operation. Note that to properly change the value of this register, the PC1 bit in CNTL1 must first be set to "0".

R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	
BUFE	BRES	BFIE	0	SMP_TH9	SMP_TH8	BUF_M1	BUF_M0	Reset Value
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	00000000
I ² C Address: 0x3Bh								

SMP_TH[9:0] Sample Threshold determines the number of samples that will trigger a watermark interrupt or will be saved prior to a trigger event. When BUF_RES=1, the maximum number of samples is 339; when BUF_RES=0, the maximum number of samples is 681.

Figure 3: KX124 SMP_TH Register/Bit Mapping

- **Sample Level (SMP_LEV)** – reports the number of data bytes that have been stored in the sample buffer
 - Sample level bits (SMP_LEV) have been expanded to 10 bits to support the larger buffer
 - Like the KX023, bits SMP_LEV[7:0] still exist in BUF_STATUS_1
 - In the KX124, the expanded bits SMP_LEV[10:8] can be found in BUF_STATUS_2[2:0]

BUF_STATUS_1

This register reports the status of the sample buffer.

R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
SMP_LEV7	SMP_LEV6	SMP_LEV5	SMP_LEV4	SMP_LEV3	SMP_LEV2	SMP_LEV1	SMP_LEV0
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
I ² C Address: 0x3Ch							

SMP_LEV[7:0] Sample Level; reports the number of data bytes that have been stored in the sample buffer. When BUF_RES=1, this count will increase by 6 for each 3-axis sample in the buffer; when BUF_RES=0, the count will increase by 3 for each 3-axis sample. If this register reads 0, no data has been stored in the buffer.

Figure 4: KX023 SMP_LEV Register/Bit Mapping

BUF_STATUS_1

This register reports the status of the sample buffer.

R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
SMP_LEV7	SMP_LEV6	SMP_LEV5	SMP_LEV4	SMP_LEV3	SMP_LEV2	SMP_LEV1	SMP_LEV0
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
I ² C Address: 0x3Ch							

BUF_STATUS_2

This register reports the status of the sample buffer trigger function.

R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
BUF_TRIG	0	0	0	0	SMP_LEV10	SMP_LEV9	SMP_LEV8
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
I ² C Address: 0x3Dh							

SMP_LEV[10:0] Sample Level; reports the number of data bytes that have been stored in the sample buffer. When BUF_RES=1, this count will increase by 6 for each 3-axis sample in the buffer; when BUF_RES=0, the count will increase by 3 for each 3-axis sample. If this register reads 0, no data has been stored in the buffer.

Figure 5: KX124 SMP_LEV Register/Bit Mapping

- WHO_AM_I Register will report a different value to discern between Kionix sensors. The KX023 will return 0x15 and KX124 will return 0x28 when reading from address 0x0F.

Part	Register	Address	Type	Value
KX023	WHO_AM_I	0x0F	Read Only	0x15
KX124	WHO_AM_I	0x0F	Read Only	0x28

- The typical *Power Up Time*, which is from VDD valid to device boot completion, varies slightly from the KX023 to the KX124. The typical time for the KX124 is 20ms vs KX023 of 10ms, however, both have a maximum limit of 50ms.

Side-by-Side Comparison

The following are key side-by-side comparisons between the KX023 and KX124 accelerometers. Typical values are shown, unless otherwise indicated.

Package Information

		KX023	KX124
Parameter	Units		
Sensing Axis (Accel)		XYZ 3-axis	XYZ 3-axis
Package Size	mm	3x3x0.9	3x3x0.9
Package Type		LGA	LGA
Pins		16	16

Features

		KX023	KX123
Parameter	Units		
Low Power Mode		Yes	Yes
Self-test		Yes	Yes
Wake-up		Yes	Yes
Freefall Detection		No	Yes
Tap, Double Tap Detection		Yes	Yes
Tilt Orientation Detection		Yes	Yes
Sample Buffer (FIFO)	Bytes	256	2048

Electrical Specifications

Parameter		Units	KX023	KX124
Supply Voltage (VDD)		V	1.71–3.6	1.71–3.6
I/O Pads Supply Voltage (IO_VDD)		V	1.7–VDD	1.7–VDD
Current Consumption	High Resolution Mode (RES = 1)	μA	145	145
	Low Power Mode (RES = 0)	μA	10	10
	Standby	μA	0.9	0.9
I2C Communication Rate (max)		MHz	3.4	3.4
SPI Communication Rate (max)		MHz	10	10

Environmental

Parameter		Units	KX023	KX124
Supply Voltage (VDD)		V	-0.3–3.63	-0.3–3.63
Operating Temperature Range		°C	-40–85	-40–85
Storage Temperature Range		°C	-55–150	-55–150
Mechanical Shock (powered and unpowered)		g	5000 for 0.5ms 10000 for 0.2ms	5000 for 0.5ms 10000 for 0.2ms
ESD (HBM)		V	2000	2000

Accelerometer Mechanical

Parameter		Units	KX023	KX124
Operating Temperature Range		°C	-40–85	-40–85
Zero-g Offset		mg	±25	±25
Zero-g Offset Variation from RT over Temp.		± mg/°C	0.2	0.2
Sensitivity	GSEL1=0, GSEL0=0 (±2g)	counts/g	16384	16384
	GSEL1=0, GSEL0=1 (±4g)	counts/g	8192	8192
	GSEL1=1, GSEL0=0 (±8g)	counts/g	4096	4096
Sensitivity Variation from RT over Temp.		%/°C	0.01	0.01
Self-Test Output change on Activation		g	0.5	0.5
Mechanical Resonance (-3dB)		Hz	3500 (xy) 1800 (z)	3500 (xy) 1800 (z)
Non-Linearity		% of FS	0.6	0.6
Cross Axis Sensitivity		%	2	2
Noise (RMS at 50Hz)		mg	0.75	0.75

Sensor Output Registers (Primary)

Addr (hex)	KX023		KX124	
	Name	Description	Name	Description
00	XHP_L	X-axis high pass filter output low	XHP_L	X-axis high pass filter output low
01	XHP_H	X-axis high pass filter output high	XHP_H	X-axis high pass filter output high
02	YHP_L	Y-axis high pass filter output low	YHP_L	Y-axis high pass filter output low
03	YHP_H	Y-axis high pass filter output high	YHP_H	Y-axis high pass filter output high
04	ZHP_L	Z-axis high pass filter output low	ZHP_L	Z-axis high pass filter output low
05	ZHP_H	Z-axis high pass filter output high	ZHP_H	Z-axis high pass filter output high
06	XOUT_L	X-axis output low	XOUT_L	X-axis output low
07	XOUT_H	X-axis output high	XOUT_H	X-axis output high
08	YOUT_L	Y-axis output low	YOUT_L	Y-axis output low
09	YOUT_H	Y-axis output high	YOUT_H	Y-axis output high
0A	ZOUT_L	Z-axis output low	ZOUT_L	Z-axis output low
0B	ZOUT_H	Z-axis output high	ZOUT_H	Z-axis output high
...
0F	WHO_AM_I	Who am I registers, returns 0x14	WHO_AM_I	Who am I register, returns 0x1B

The Kionix Advantage

Kionix technology provides for X, Y, and Z-axis sensing on a single, silicon chip. One accelerometer can be used to enable a variety of simultaneous features including, but not limited to:

- Hard Disk Drive protection
- Vibration analysis
- Tilt screen navigation
- Sports modeling
- Theft, man-down, accident alarm
- Image stability, screen orientation & scrolling
- Computer pointer
- Navigation, mapping
- Game playing
- Automatic sleep mode

Theory of Operation

Kionix MEMS linear tri-axis accelerometers function on the principle of differential capacitance. Acceleration causes displacement of a silicon structure resulting in a change in capacitance. A signal-conditioning CMOS technology ASIC detects and transforms changes in capacitance into an analog output voltage, which is proportional to acceleration. These outputs can then be sent to a micro-controller for integration into various applications.

For product summaries, specifications, and schematics, please refer to the Kionix MEMS accelerometer product sheets at <http://www.kionix.com/parametric/Accelerometers>