Utilizing the Power Shutdown Capabilities of the Kionix Tri-Axis Accelerometers

Introduction

Kionix tri-axis accelerometers feature a power shutdown capability. Even with their typically low current draw, there are still applications that may require even less power consumption. For these applications, it is possible to implement a duty-cycle power-reduction methodology that uses a microprocessor to toggle the Enable/Disable pin or register at a specified duty-cycle. This approach can reduce greatly the accelerometer's current draw during the majority of its time in operation. This application note provides the theory and equations needed to take full advantage of this power saving capability.

Power Shutdown Methodology

There are a few questions that must be addressed when determining what duty-cycle power-reduction parameters to use. This is because the required bandwidth, BW, is determined by and impacts them all:

- What is the target application?
- What would you like to measure?
- How quickly do you need to sense changes in acceleration?
- What is the desired resolution?

The low-pass filter capacitor can be thought of as a time delay that delays the output response of an acceleration input. The lower the bandwidth, the longer the delay and startup time. Therefore, limiting the maximum sampling rate for the application. The desired bandwidth and the resulting startup time, $T_{startup}$, can be calculated using Equation 1.

$$BW = \frac{1}{2\pi RC}$$

$$T_{startup} = 5*RC$$

Equation 1: Bandwidth (Hz) and Startup Time (ms), R = output resistance (Ω), C = filter capacitance (μf)

Resolution improves with a lower bandwidth; therefore, a requirement for more resolution will result in a slower response and longer startup time. Resolution can be calculated using Equation 2.

$$\text{Resolution} = N * \sqrt{BW * 1.6}$$

Equation 2: Resolution (mg), N = noise density ($\frac{\mu g}{\sqrt{Hz}}$), BW = Bandwidth (Hz)

Once the required bandwidth and resolution are determined, the final maximum sampling rate can be calculated. Startup time, $T_{startup}$, combined with the microprocessor's sampling and A/D conversion time, determines how long the power shutdown pin needs to be held at

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Vdd to get an accurate reading. This is also known as the power on time, $T_{on.}$ Note that since the microprocessor's sample and A/D conversion time is much smaller that $T_{startup}$, multiple accelerometer readings could be taken during this time period with minimal effect on the final maximum sample rate.

The duty-cycle and T_{on} are used to determine the period of the power shutdown toggle. Finally, the maximum sampling rate is determined by taking the inverse of the period of the sample time, as shown in Equation 3.

$$\text{Period} = \frac{T_{on}}{Duty - Cycle}$$

$$\text{Sampling Rate} = \frac{1}{Period}$$

Equation 3: Period (ms) and Maximum Sampling Rate (Hz), T_{on} (ms), Duty-Cycle (%)

Microprocessor Controlled Power Reduction System

When the Kionix accelerometer is hooked up to a microprocessor, such as the Texas Instruments MSP430F149, a 10% duty-cycle, power shutdown toggled system can be easily implemented. This power-reduced system will decrease the accelerometer's typical current draw by 90%. Note that a reduction in current draw also means limitations to maximum sampling rate.

The TI MSP430F149 can sample and complete an A/D conversion of all three accelerometer outputs in 12.6µs. For example, when running with a bandwidth of 500Hz, this would yield a final T_{on} of 1.6126ms. Therefore, with a 10% duty-cycle, and a period of 16.126ms, the Enable pin will be grounded for 14.5134ms. The timing diagram in Figure 1 illustrates this duty-cycle toggling of the Enable pin.

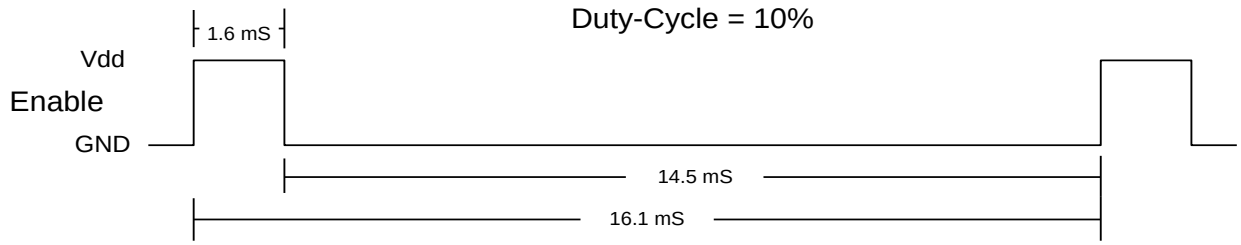

Figure 1: Power Shutdown Timing Diagram

Finally, the period is used to determine that the maximum tri-axis sampling rate for this system is 62 Hz. Note that bandwidth and duty-cycle can be varied to provide a sufficient sampling rate for the chosen application. Figure 2 shows the expected tri-axis sampling rate for a variety of bandwidths when utilizing a 10% duty-cycled, power-reduction methodology.

Bandwidth (Hz)	X,Y Res (mg)	Z Res (mg)	Max Sampling Rate (Hz)
50	0.31	0.58	6
500	0.99	1.84	62
1500	1.71	3.18	188

Figure 2: Sampling Rate Table

When implementing this power reduction system, the simple flow chart in Figure 3 can be used as a guideline for programming a microprocessor to toggle the power shutdown pin.

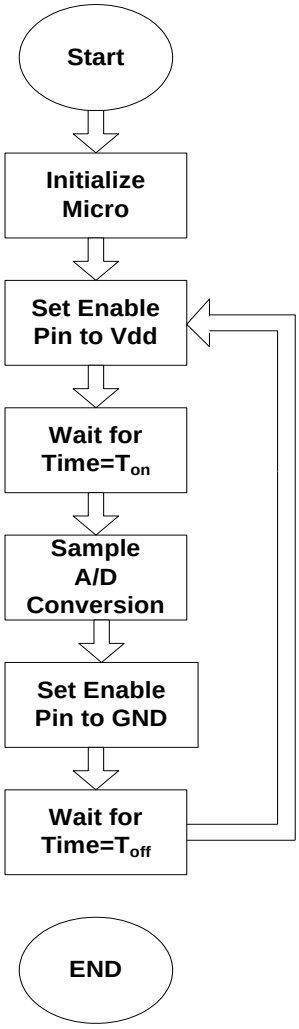

Figure 3: Power Shutdown Flow Chart

Theory of Operation

Kionix MEMS linear tri-axis accelerometers function on the principle of differential capacitance. Acceleration causes displacement of a silicon structure resulting in a change in capacitance. A signal-conditioning CMOS technology ASIC detects and transforms changes in capacitance into an analog output voltage which is proportional to acceleration. These outputs can then be sent to a micro-controller for integration into various applications. Kionix technology provides for X, Y and Z-axis sensing on a single, silicon chip. One accelerometer can be used to enable a variety of simultaneous features including, but not limited to:

Drop force modeling for warranty management
Hard disk drive shock protection
Tilt screen navigation
Theft, man-down, accident alarm
Image stability, screen orientation
Computer pointer
Navigation, mapping
Game playing

For product summaries, specifications, and schematics, please refer to the Kionix accelerometer product sheets at http://www.kionix.com/parametric/Accelerometers.